11 Muon trigger for the barrel

11.1 Hardware description of the system

As already described in Chapters 9 and 10, the level-1 muon trigger makes use of dedicated RPC detectors in the barrel region [11-1]. The trigger processing includes a low-p_T trigger and a high-p_T trigger [11-2]–[11-7]. To reduce the rate of accidental triggers, due to low-energy background particles in the ATLAS cavern, the algorithm is performed in both the η and ϕ projections for both low-p_T and high-p_T triggers. A valid trigger is generated only if the trigger conditions are satisfied for both projections. In addition, the ϕ projection gives to the experiment the second muon coordinate with a resolution of 1 cm.

As shown in Figure 11-1, the low-p_T algorithm makes use of information generated from the

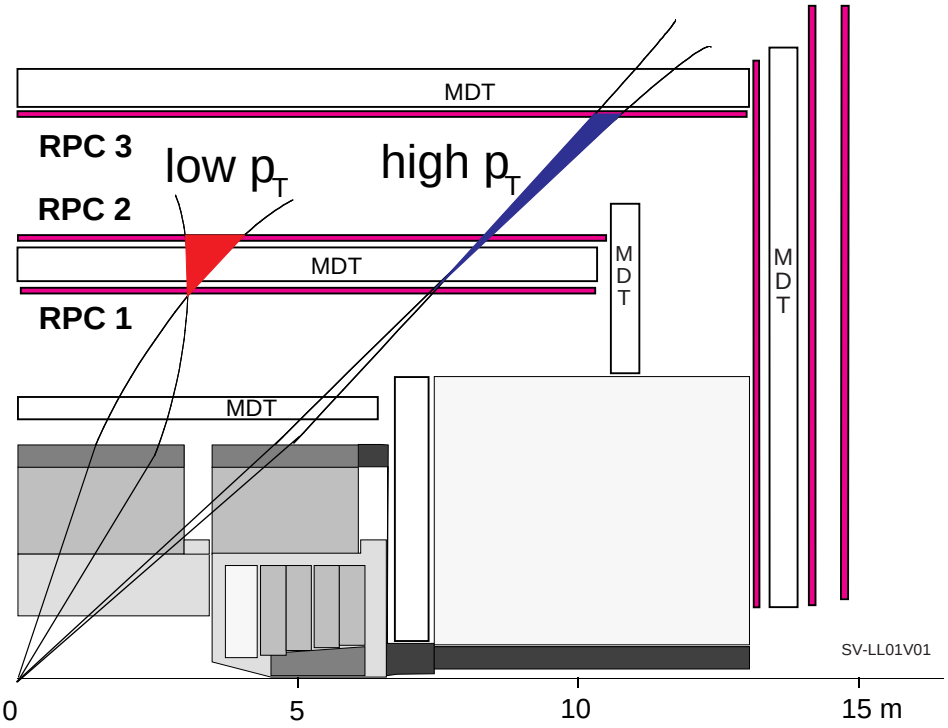

Figure 11-1 Schematic view of the trigger principle.

two Barrel Middle (BM) RPC1 and RPC2 stations. Each station is made of two RPC doublets, one in the η (bending) projection and one in the ϕ (non-bending) projection, and the first stage of the trigger algorithm is performed separately and independently for the two projections [11-8].

The algorithm operates in the following way: if a track hit is generated in the first RPC1 doublet (so-called pivot plane), a search for the same track is made in the second RPC2 doublet, within a road whose centre is defined by the line of conjunction of the hit in the first doublet with the interaction point. The width of the cone is a function of the desired cut on p_T: the smaller the

cone, the higher the cut on p_T. The system is designed so that three p_T thresholds in each projection can be applied simultaneously. In addition, to cope with background from low-energy particles in the cavern, a 3/4 majority coincidence of the four hits of the two doublets is required [11-9].

The η and ϕ trigger information is combined to generate the so-called 'Regions-of-Interest' (RoI), identifying areas in the apparatus in which valid triggers were produced with a spatial resolution of ~ 0.1 × 0.1 in η-ϕ.

The high-p_T algorithm makes use of the result of the low-p_T trigger and of the information generated in the RPC3 Barrel Outer (BO) station. This station is made of two RPC doublets, one in the η projection and one in the ϕ projection. The algorithm operates in a similar way to the low-p_T one. The centre of the road is determined in the same way as for the low-p_T trigger and a 1/2 majority coincidence of the RPC3 doublet and of the low-p_T trigger pattern result is required. As for the low-p_T trigger, three p_T thresholds operate simultaneously and a 0.1 × 0.1 η-ϕ RoI is generated.

11.1.1 Overview of the electronics system

As discussed in Chapter 10, the signals from the RPC detector are amplified, discriminated and digitally shaped on the detector. The Amplifier–Shaper–Discriminator (ASD) boards, each containing eight ADS channels, are attached to the chamber at the end of the RPC strips.

Figure 11-2 shows the context diagram of the overall trigger and read-out system, indicating which of the two main functionalities each board performs.

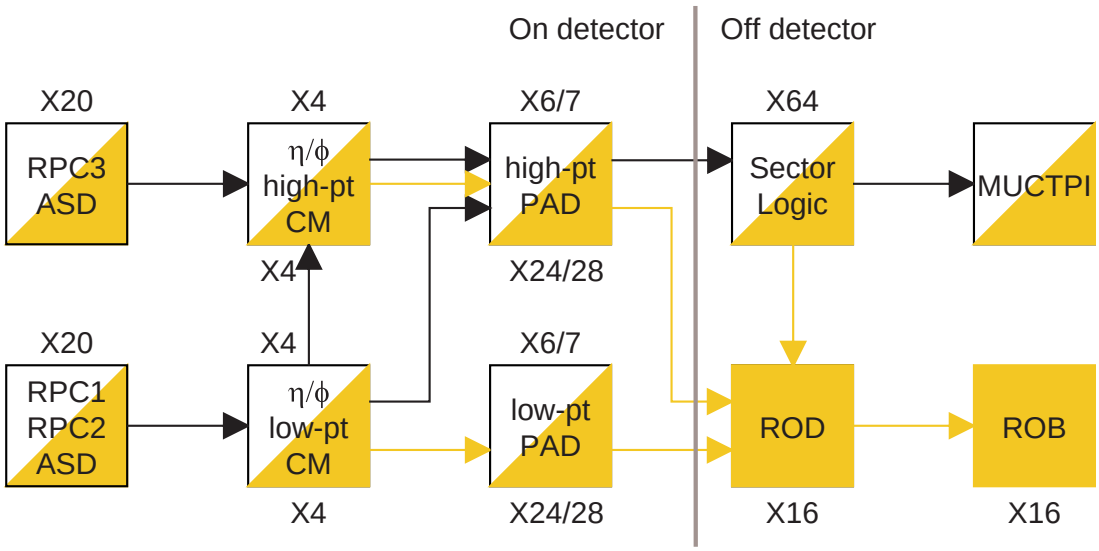

Figure 11-2 Context diagram of the barrel RPC trigger system. Each system component functionality is also indicated (white for trigger, grey for read-out and white/grey for trigger and read-out functionality.

In the low-p_T trigger, for each of the η and the ϕ projections, the RPC signals of the two detector doublets, RPC1 and RPC2, are sent to a Coincidence-matrix (CM) board, that contains a CM chip. This chip performs almost all of the functions needed for the trigger algorithm and also for the read-out of the strips. It aligns the timing of the input signals, performs the coincidence and

majority operations, and makes the p_T cut on three different thresholds. It also contains the level-1 latency pipeline memory and derandomizing buffer. A detailed description of the chip is given in Section 11.1.3.1.

The CM board produces an output pattern containing the low-p_T trigger results for each pair of RPC doublets in the η or ϕ projection. The information of two adjacent CM boards in the η projection, and the corresponding information of the two CM boards in the ϕ projection, are combined together in the low-p_T Pad Logic (Pad) board. The four low-p_T CM boards and the corresponding Pad board are mounted on top of the RPC2 detector, as shown schematically in Figure 11-3.

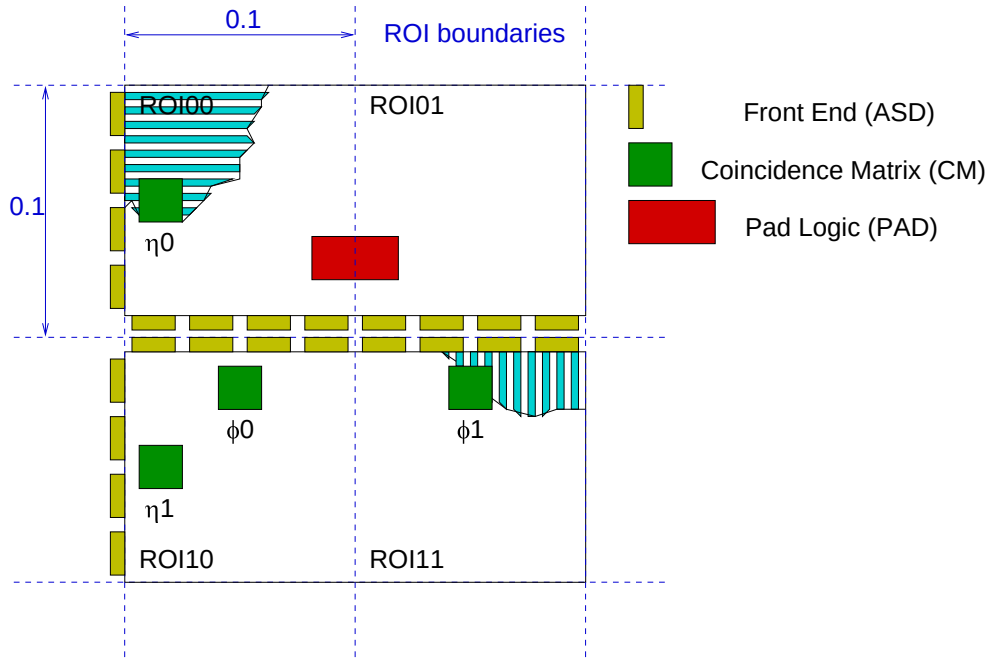

Figure 11-3 On-detector electronics for low- and high-p_T triggers.

The low-p_T Pad board generates the low-p_T trigger result and the associated RoI information. This information is transferred, synchronously at 40MHz, to the corresponding high-p_T Pad board, that collects the overall result for low- and high-p_T.

In the high-p_T trigger, for each of the η and ϕ projections, the RPC signals from the RPC3 doublet, and the corresponding pattern result of the low-p_T trigger, are sent to a CM board, very similar to the one used in the low-p_T trigger. This board contains the same coincidence-matrix chip as in the low-p_T board, programmed for the high-p_T algorithm. The high-p_T CM board produces an output pattern containing the high-p_T trigger results for a given RPC doublet in the η or ϕ projection. The information of two adjacent CM boards in the η projection and the corresponding information of the two CM boards in the ϕ projection are combined in the high-p_T Pad Logic board. The four high-p_T CM boards and the corresponding Pad board are mounted on top of the RPC3 detector.

The high-p_T Pad board combines the low- and high-p_T trigger results. The combined information is sent, synchronously at 40MHz, via optical links, to a Sector Logic (SL) board, located in the USA15 counting room. Each SL board receives inputs from seven (six) low-p_T (high-p_T) Pad boards, combining and encoding the trigger results of one of the 64 sectors into

which the barrel trigger system is subdivided. The trigger data elaborated by the Sector Logic is sent, again synchronously at 40MHz, to the Muon Interface to the Central Trigger Processor (MUCTPI), located in the same counting room.

Data are read out from both the low- and high-p_T Pad boards. These data include the RPC strip pattern and some additional information used in the LVL2 trigger. The read-out data for events accepted by the LVL1 trigger are sent asynchronously to Read-Out Drivers (RODs) located in the USA15 underground counting room and from here to the Read-Out Buffers (ROBs). The data links for the read-out data are independent of the ones used to transfer partial trigger results to the SL boards.

Pad, SL and MUCTPI modules generate themselves read-out data on partial trigger results, in order to monitor the system.

11.1.2 System segmentation

From the trigger point of view, the barrel system is segmented into 64 logically (but not physically) identical sectors.

The barrel is divided in two parts, $\eta<0$ and $\eta>0$. Within each half barrel, 32 sectors are defined. The correspondence between these logical sectors and physical chambers is indicated in Figure 11-4. The Barrel Large (BL) chambers and the Barrel Small (BS) chambers of both middle and outer RPC stations are logically divided in two to produce two large sectors and two small sectors per half-barrel octant.

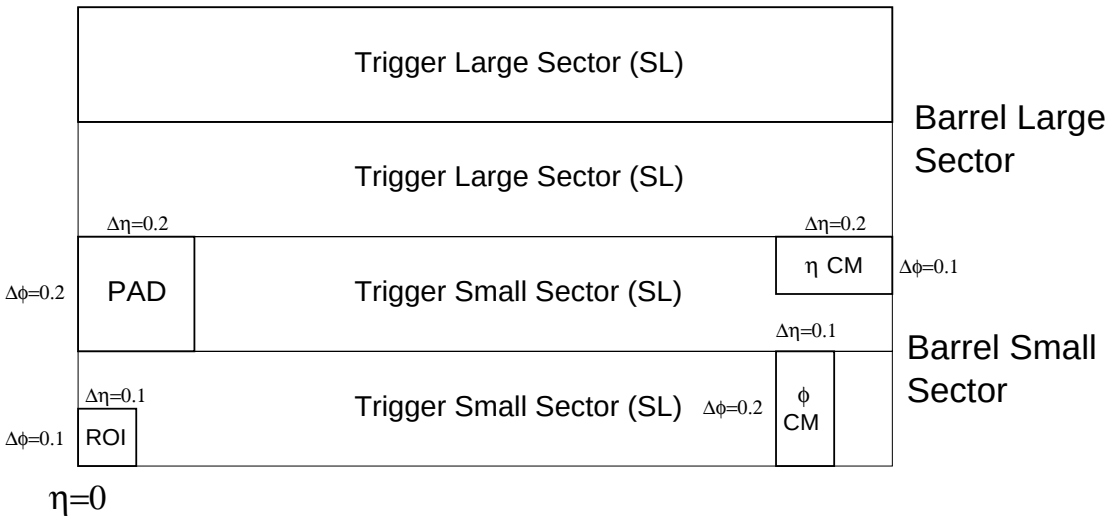

Figure 11-4 Barrel trigger segmentation. Also indicated in the figure are the areas covered by η and φ CM boards, by an RoI, by a Pad Logic (PL) board and by a Sector Logic (SL) board.

Inside a sector, the trigger is segmented in Pads and RoIs. The Pad segmentation is different for large and small sectors; this difference follows the muon spectrometer layout. Two relevant factors that affect the performance and implementation of the trigger system were taken into account in the segmentation: the RPC strip length and the front-end modularity.

The strip should not be too long (the length never exceeds 2.5 m in the bending projection) to avoid a large spread in the signal propagation delay that would make the bunch-crossing identification (BCID) difficult or impossible.

Concerning the front-end modularity, the basic segmentation is 32 channels (two sets of 32 inputs received per RPC doublet) generated by four eight-channel ASD boards. This makes it possible to have the same dimension of the coincidence-matrix inputs in all the apparatus and an easier cabling of the system. Because of layout constraints, in some part of the apparatus it was impossible to follow this segmentation. To handle this case, the CM chip can be programmed to simulate inputs that do not exist.

A large sector contains six Pad regions, while a small sector contains seven Pad regions. Table 11-1 gives the total number of each type of RPC chamber, used in the barrel trigger. The number of strips per chamber is matched to the CM dimensions. The strip length is chosen to give a maximum propagation delay spread of ±7 ns.

Table 11-1 Number of RPC chambers of each type used in the barrel trigger (dimensions in mm).

Name	Nº. chamber	η pitch	η strip length	Nº. chan / chamber	Nº. chan.	ϕ pitch	ϕ strip length	Nº. chan. / chamber	Nº. chan.
BMSa	144	30.0	1480	24	13824	23.1	720	128	36864
BMSb	96	26.2	1480	32	12288	23.1	840	128	24576
BMSc	24	30.0	1480	32	3072	23.1	960	128	6144
BMFa	16	30.0	1480	24	1536	23.1	720	128	4096
BMFb	16	30.0	1480	32	2048	23.1	960	128	4096
BMFc	16	33.8	1480	32	2048	23.1	1080	128	4096
BOSa	8	26.2	1830	32	1024	25.4	840	144	2304
BOSb	16	30.0	1830	32	2048	25.4	960	144	4608
BOSc	120	27.0	1830	40	19200	25.4	1080	144	34560
BOFa	16	30.0	1830	24	1536	25.4	720	144	4608
BOFb	8	30.0	1830	32	1024	25.4	960	144	2304
BOFc	8	27.0	1830	40	1280	25.4	1080	144	2304
BOHa	18	30.0	970	40	1440	24.2	1200	40	1440
BOGa	18	30.0	1105	40	2880	25.1	1200	88	3168
BMLa	64	30.0	1720	24	6144	26.8	720	128	16384
BMLb	192	26.0	1720	32	24576	26.8	840	128	49152
BMLc	64	37.5	1720	32	8192	26.8	1200	128	16384
BML1	16	30.0	1720	16	1024	26.8	480	128	4096
BOLa	16	26.2	2425	32	8192	25.3	840	192	24576
BOLb	128	27.0	2425	40	20480	25.3	1080	192	49152

The region covered by a Pad is ~ 0.2×0.2 in $\Delta\eta \times \Delta\phi$. Inside the Pad the trigger is segmented into RoIs. An RoI is a region given by the overlap of an η coincidence-matrix and a ϕ coincidence-matrix. The dimension of the RoI is ~ 0.1×0.1 in $\Delta\eta \times \Delta\phi$.

The total number of Pads is $7 \times 2 \times 32$ for the small sectors and $6 \times 2 \times 32$ for the large ones, giving 416 Pads altogether. Since one Pad covers four RoIs, the total number of RoIs is 1664.

Concerning system segmentation, a relevant issue is the overlap handling [11-10]. Overlap between different parts of the apparatus cannot be avoided without losing efficiency in the trigger system due to uncovered regions. On the other end, overlap can cause double counting of muon candidates. (The same muon can be counted twice, by adjacent parts of the apparatus.) In the barrel trigger system, overlap is treated and solved at three different levels (Figure 11-5).

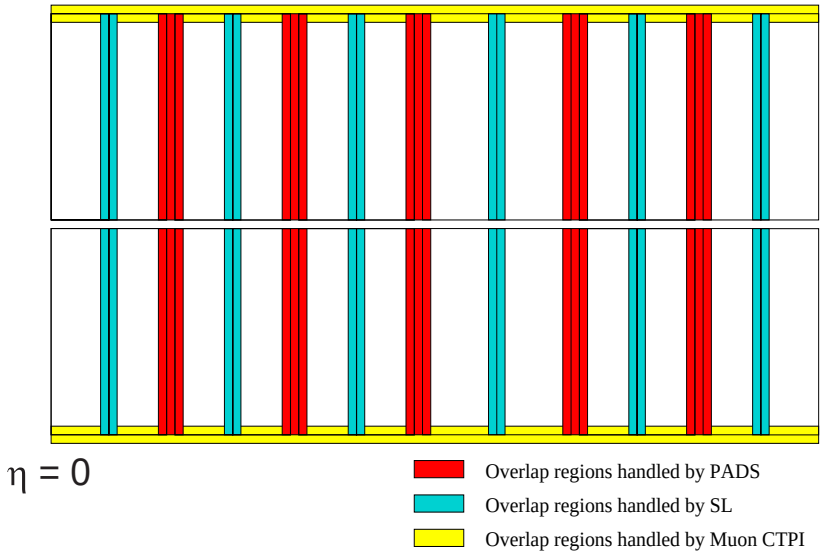

Figure 11-5 Overlap handling.

11.1.2.1 Overlap handling

Overlap within a Pad region

The problem of overlap inside a Pad region is solved by the Pad Logic that removes double counting of tracks between the four RoIs of the region. In addition, if it is found that a trigger was generated in a zone of overlap with another Pad region, this trigger is flagged as ‘border’ trigger and any overlap will be solved later on by the Sector Logic or by the MUCTPI.

Overlap within a sector

As stated above, the triggers generated in a zone of overlap between different Pads are flagged by the Pad logic and sent to the Sector Logic; the Sector Logic prevents double counting of triggers inside a sector. In addition, if it is found that a trigger was generated in a zone of overlap with another sector of the barrel or the end-cap, this trigger is flagged as a ‘border’ trigger and the overlap will be solved later on by the MUCTPI.

Overlap between sectors

Triggers generated in zones of overlap between different Sectors are flagged by the Sector Logic and sent to the MUCTPI which prevents double counting between sectors.

11.1.3 Coincidence-matrix board

The CM board performs almost all of the functions needed for the trigger algorithm and for the read-out of the system. It receives the signals from the RPC doublets and performs the trigger algorithm and read-out functions using a dedicated coincidence-matrix chip. Two separate boards make the low- and high-p_T triggers, using the same CM chip programmed in a different way. In terms of connections to the rest of the system (see Section 11.1.8), both boards have a separate connection to the read-out system, via the RODs (Figure 11-15), while the trigger information of the low-p_T and high-p_T is concentrated on the high-p_T board and then sent to the Sector Logic (Figure 11-17).

11.1.3.1 The coincidence-matrix chip

This chip performs most of the functions needed for the low-p_T and high-p_T triggers and for the read-out [11-11]. These functions are:

- timing and digital shaping of the signals coming from the RPC doublets.
- execution of the trigger algorithm.
- data storage during LVL1 latency.
- trigger and read-out data generation.
- storage of read-out data in derandomizing memory.

Figure 11-6 shows a block diagram of the coincidence-matrix chip. The chip receives the 40 MHz machine clock and through a Delay Locked Loop (DLL) system, it generates a 320 MHz internal clock that synchronizes all the pipeline operations inside the chip.

The estimated dimension of the matrix is 32×48 inputs. In the low-p_T trigger, the signals coming from the RPC1 doublet are connected to the 32 I0 and 32 I1 inputs, and the signals coming from the RPC2 doublet are connected to the 48 J1 and 48 J2 inputs. In the case of the high-p_T trigger the I0 inputs are used to connect the low-p_T trigger result (the I1 inputs are not used), while the J0 and J1 inputs are both used to connect the high-p_T RPC doublet.

The first block at the input of the chip is an edge detector and dead-time circuit. This block detects the rising edge of the arriving signals and, for each detected signal, sets a programmable dead time, of the order of a few hundred nanoseconds, to avoid the arrival of extra pulses in the same RPC channel.

The second block at the inputs allows for the possibility of masking RPC noisy channels.

The third input block is a programmable-depth pipeline that is very important for setting up the timing of the system. Since the cables that bring the signals to the chip could have different lengths, corresponding to different paths, this block allows for timing adjustment of the different groups of signals in such a way that their coincidence is in time. The pipeline can be programmed in groups of eight RPC signals, with a minimum step corresponding to the period

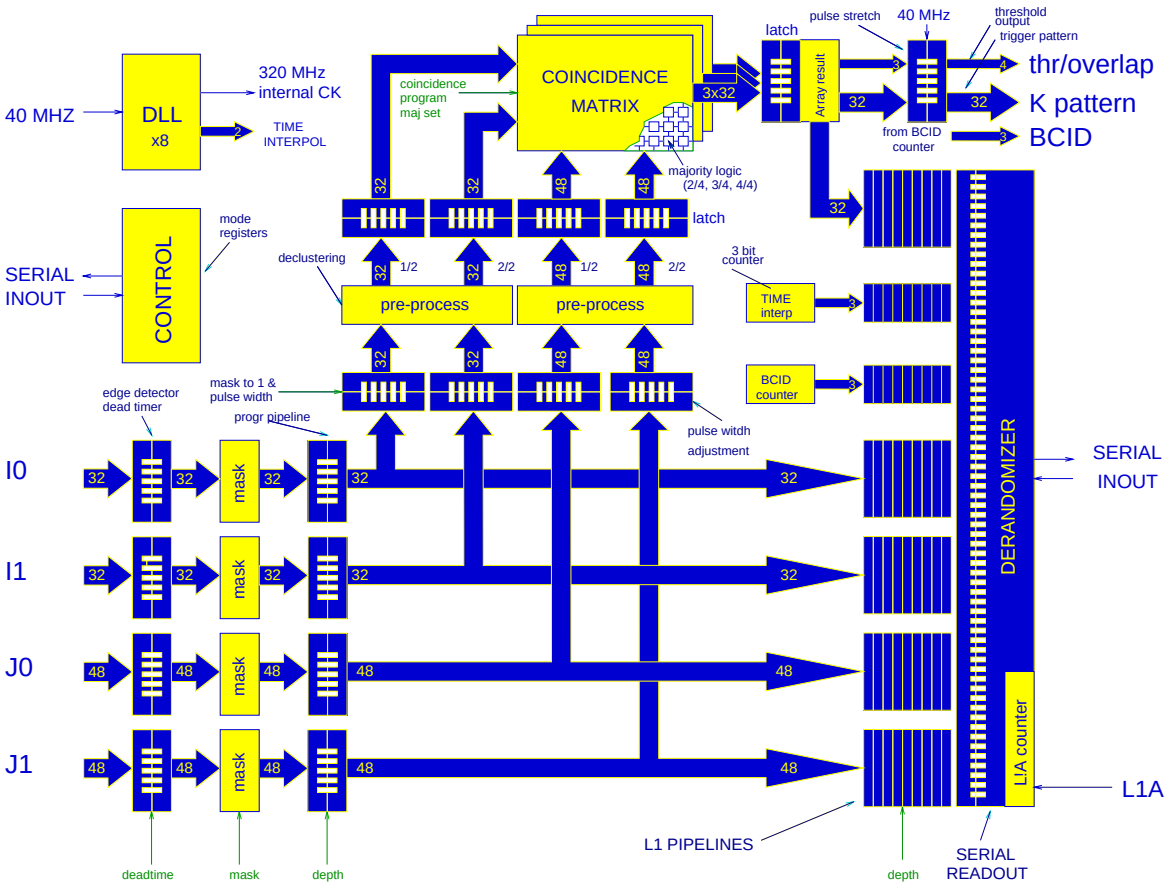

Figure 11-6 Coincidence-matrix chip block diagram.

of the 320 MHz internal clock (~ 3.1 ns). The RPC front-end takes care of aligning in time a group of eight signals, with a maximum spread of 0.5 ns.

At the output of the programmable-depth pipeline, the signals follow two different paths: one to the read-out part and one to the trigger part.

In the trigger part, the first block is the ‘mask to 1 and pulse width’. This block allows for masking to ‘1’ unused inputs to the matrix and for the digital shaping of the signal before making the trigger coincidence. Digital shaping is necessary since the signals must be made as short as possible before the coincidence, to minimize the rate of fake triggers due to low-energy background particles in the ATLAS cavern (uncorrelated noise). This block allows for a programmable digital shaping of the signals, adjusting the duration in steps of ~3.1 ns, corresponding to the internal clock period.

The next block is the preprocessing block. Here the declustering of the signals and the 1/2 and 2/2 majority logic are performed. The RPC detector has an intrinsic cluster size of about 1.5 strips and a declustering algorithm is needed to define the cluster centre.

A latch follows the pre-processing block. This circuit sets the timing at the input of the coincidence-matrix.

The coincidence-matrix has three times 32×48 cells, since the trigger must be performed on three different p_T thresholds simultaneously. The cells have the possibility to be programmed at

will, through a dedicated serial line, to perform 2/4, 3/4, or 4/4 majority logic, and to be set according to the required cut on the p_T threshold.

The output of the coincidence-matrix is sent to the read-out part, and to the trigger output part of the chip. Before producing the trigger output, the trigger pattern is synchronized back to the 40 MHz machine clock.

The trigger result (total of 39 bits) is produced synchronously at 40 MHz. The 32-bit 'K pattern' contains the RPC1 doublet pattern that has generated the trigger. Two bits are used for coding the highest p_T threshold that was validated by the trigger (in case of no trigger both bits are zero), and two bits are used as a flag to indicate whether the trigger occurred in a possible overlap zone (left or right) within the Pad region. The remaining three bits contain the low-order bits of the BCID number.

The main element in the read-out part of the chip is the level-1 pipeline memory. This memory stores the information for a time corresponding to the ATLAS level-1 trigger latency, which is 2.5μs, including some reserve. Since the memory is clocked at 320 MHz, to reach 2.5 μs of latency the depth of the memory must be ~ 800 steps.

The level-1 latency memory is subdivided in seven blocks: two 48-bit blocks and two 32-bit blocks contain the information from the RPC doublets; one 32-bit block contains the trigger array output result; one 3-bit block contains the BCID counter. The last block contains a 3-bit time interpolator that gives the subdivision by eight of the period and tells the read-out at which moment, within the period, the trigger occurred. This information is needed for the timing calibration of the system (see Section 11.2.4.1).

For events selected by the LVL1 trigger, the data from the level-1 latency memory are transferred to the derandomizing memory from here they are read out serially.

The coincidence-matrix chip will be designed in 0.25μm CMOS technology that has some desirable features for the design of the chip. The technology is radiation tolerant for the levels of neutron and gamma radiation (~10 krad over 10 years) expected in the muon spectrometer. In addition, the deep sub-micron technology allows the 320 MHz working frequency, necessary to maintain the design performances of the trigger. Another relevant issue of this technology, is the low-voltage supply that allows for reduced power consumption. This is very important in the design of the barrel system, since the goal is to put the electronics on the detector without any cooling. Table 11-2 gives the relevant chip specifications.

Table 11-2 Coincidence-matrix chip specifications

Number of logic gates	~ 120000
Memory dimension	~ 120 kbit
External clock	40 MHz
Internal working frequency	320 MHz
Power dissipation	< 1 W max
Number of I/Os	~ 210
Package type	BGA

11.1.4 Low-p_T coincidence-matrix board

The low-p_T CM board performs the low-p_T trigger algorithm in the η or in the φ projection. Figure 11-7 shows a block diagram of the board. IL0 and IL1 are the front-end signals from the RPC1 doublet, and JL0 and JL1 are the front-end signals from the RPC2 doublet. The signals are transmitted from the front-end electronics to the board in Low Voltage Differential Signalling

(LVDS) standard. The signals enter the board via LVDS receivers, where they are translated into CMOS signals, suitable for the CM chip inputs.

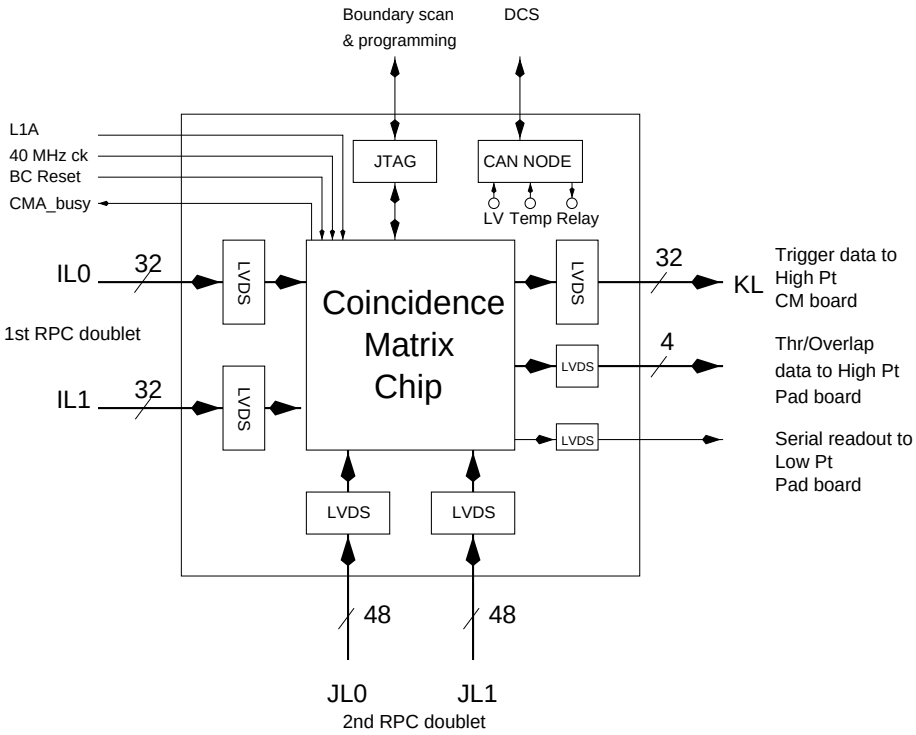

Figure 11-7 Block diagram of the low-p_T coincidence-matrix board.

As already explained above, the trigger algorithm and read-out functions are performed in the coincidence-matrix chip. The chip produces the 32-bit KL trigger pattern to be transmitted to the high-p_T coincidence-matrix board and the 4-bit trigger data pattern to be transmitted to the high-p_T Pad board. The read-out information is transmitted serially to the low-p_T Pad board. All output signals are in LVDS standard.

The CM boards of the ϕ projections must also take into account the bending in the η projection. Since no p_T cut is imposed on the ϕ projection, and since the muon tracks of low momentum can spread over more than one chamber, the OR-ing of the 48 JL0 and JL1 inputs with the corresponding inputs of the adjacent matrices is required, as shown in Figure 11-8.

The control and programming functions of the board are performed by the I2C interface and by the Detector Control System (DCS CAN node). The I2C interface allows programming of the functions inside the coincidence-matrix chip and checking of the functionalities of the circuits through the boundary-scan facility.

The board also receives the Level-1 Accept (L1A), the machine clock and the Bunch-Crossing Reset (BCR) signals of the ATLAS Timing, Trigger and Control System (TTC). It produces a CM Busy (CM_BUSY) signal that is sent back to the Pad Logic to indicated if the derandomizer buffer of the chip is almost full.

The DCS system monitors the temperature of the board and the low-voltage supply. If necessary, the system can switch off the board through a relay. The DCS is based on the use of the CAN field-bus standard, following ATLAS policy.

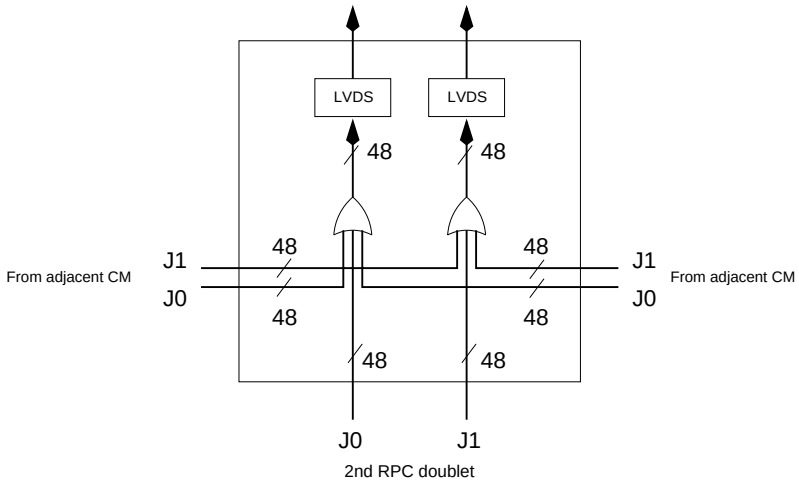

Figure 11-8 Input circuit for the ϕ low- and high-p_T CM boards.

11.1.5 High-p_T coincidence-matrix board

The high-p_T CM board performs the high-p_T trigger algorithm in the η or in the ϕ projection. Figure 11-9 shows a block diagram of the board. The IH input is the pattern result (KL) of the low-p_T trigger, and the JH1 and JH2 inputs are the front-end signals from the RPC3 doublet. The signals are transmitted in LVDS standard and then translated into CMOS signals, suitable for the coincidence-matrix chip inputs.

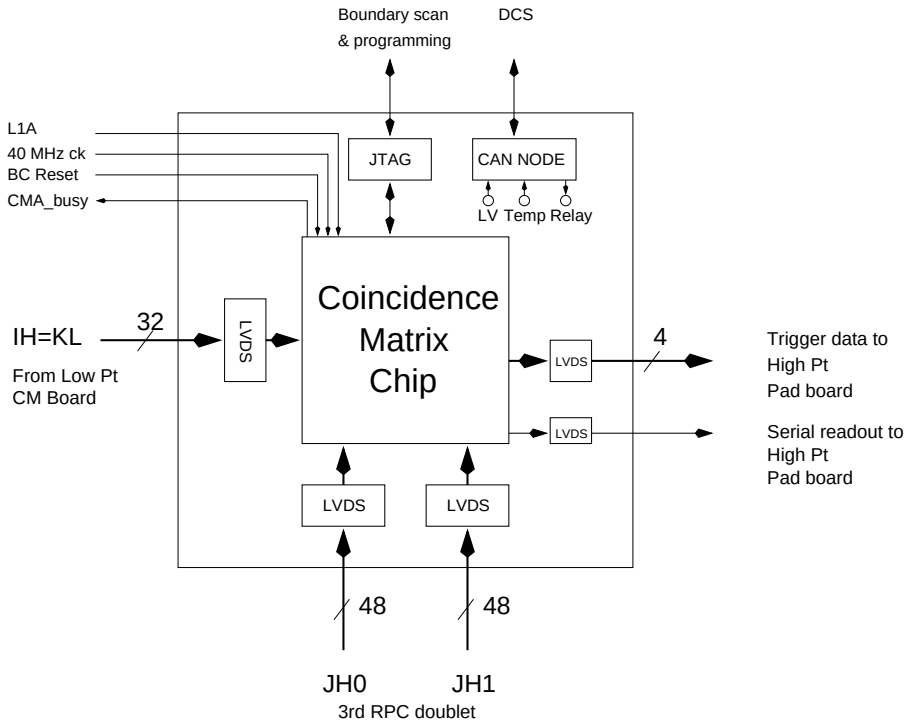

Figure 11-9 Block diagram of the high-p_T coincidence-matrix board.

As for the low-p_T board, the trigger algorithm and read-out functions are performed in the coincidence-matrix chip. The chip produces the 4-bit trigger data and the serial read-out information to be transmitted to the high-p_T Pad board.

All the functions of the board are performed in the same way as for the low-p_T board.

11.1.6 Pad logic board

The information from two adjacent CM boards in the η projection and the information from the two corresponding CM boards in the ϕ projection are combined in the Pad Logic (PL) board. Two different PL boards will be used: one for the low-p_T trigger and one for the high-p_T one. The low-p_T PL board is much simpler than the high-p_T PL board. It only combines the low-p_T read-out information of the two η and two ϕ low-p_T CM boards. The high-p_T PL board combines the high-p_T read-out information of the two η and two ϕ high-p_T CM boards and, in addition, it combines all of the trigger information generated by the four low-p_T CM boards and the four high-p_T CM boards.

The design of the PL board is based on a dedicated gate-array ASIC, developed in radiation-tolerant technology. Although the functions required for the low-p_T PL board are much simpler than those required for the high-p_T PL board, the design of both is based on the same chip, to avoid the overheads and costs of developing two circuits.

11.1.6.1 Pad-logic chip

The most important functions performed by the chip are the combination of the trigger information and of the read-out information from the four CM boards connected to the Pad. The logic associated with these two functions is described below.

PL chip read-out logic

The combination of the read-out information is shown in Figure 11-10. The four serial inputs of the two η and two ϕ matrices are transformed into parallel patterns and then combined together and formatted. The combined pattern is retransformed into a bit-stream suitable for serial transmission to the ROD.

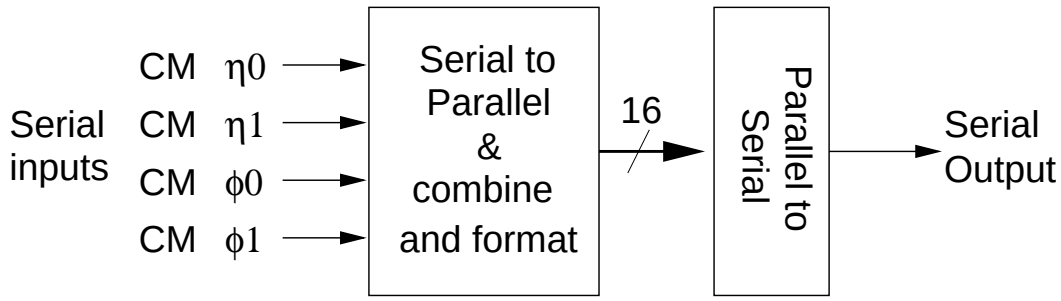

Figure 11-10 Block diagram of the PL chip read-out logic.

PL chip trigger logic

The Pad chip trigger logic combines the low- and high-p_T trigger information in the η and φ projections, assigning track candidates to RoIs. It also deals with the overlap inside the Pad region and tags possible ambiguities in case of more than one track in the region.

Table 11-3 pad-logic trigger output

Bit	Description
0-1	RoI number inside the Pad region
2-5	p_T coding (three low-p_T thresholds + three high-p_T thresholds)
6	Overlap φ flag to be solved by the MUCTPI
7	Overlap η flag to be solved by the Sector Logi
8-9	Ambiguity bits to be sent only to the read-out

The Pad trigger logic is shown in Figure 11-11. The logic works in pipeline mode at the machine clock frequency. The operations are performed in three pipeline steps. In the first step the input trigger data coming from the CMs is aligned in time. In the second step the highest threshold is found and the pad overlaps are solved independently for each projection. Overlap and ambiguity flags are set at this stage. During the third step the two views are combined and the 10-bit output word is produced.

The trigger logic receives as input eight times four bits coming from the four low-p_T coincidence-matrices (two per projection) and the four high-p_T coincidence-matrices.

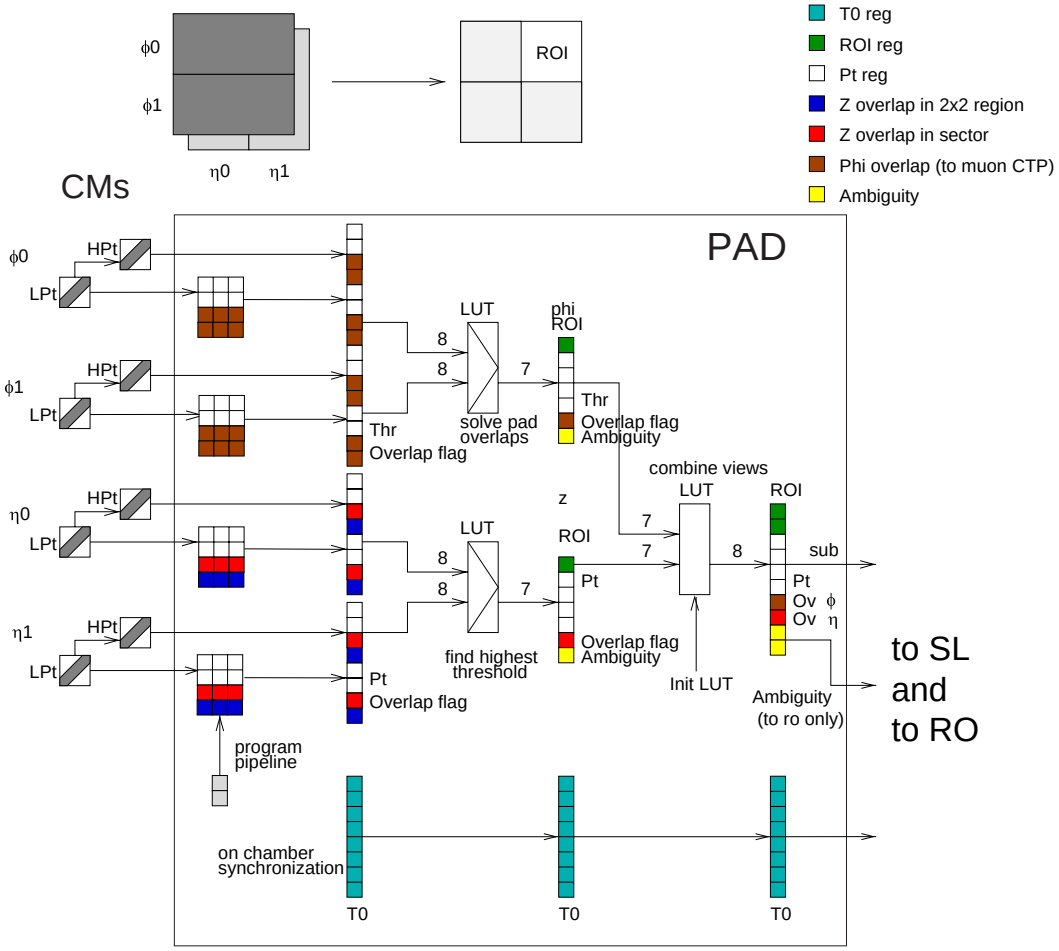

Figure 11-11 Block diagram of the Pad chip trigger logic.

The trigger logic produces a ten-bit output pattern. Eight bits are sent to the trigger Sector Logic, while the full ten bits are sent to the read-out. The content of the output pattern is illustrated in Table 11-3. In case of more than one muon candidate in the pad region, the logic transfers only the highest-p_T candidate and informs the level-2 trigger of the possibility of a second candidate using the ambiguity bits.

11.1.6.2 The Low-p_T Pad-Logic board

The low-p_T pad board combines the read-out information of two η and two ϕ low-p_T CM boards using the read-out logic part of the pad logic chip described above. A block diagram of the low-p_T Pad board is shown in Figure 11-12. The read-out input data are received serially from the

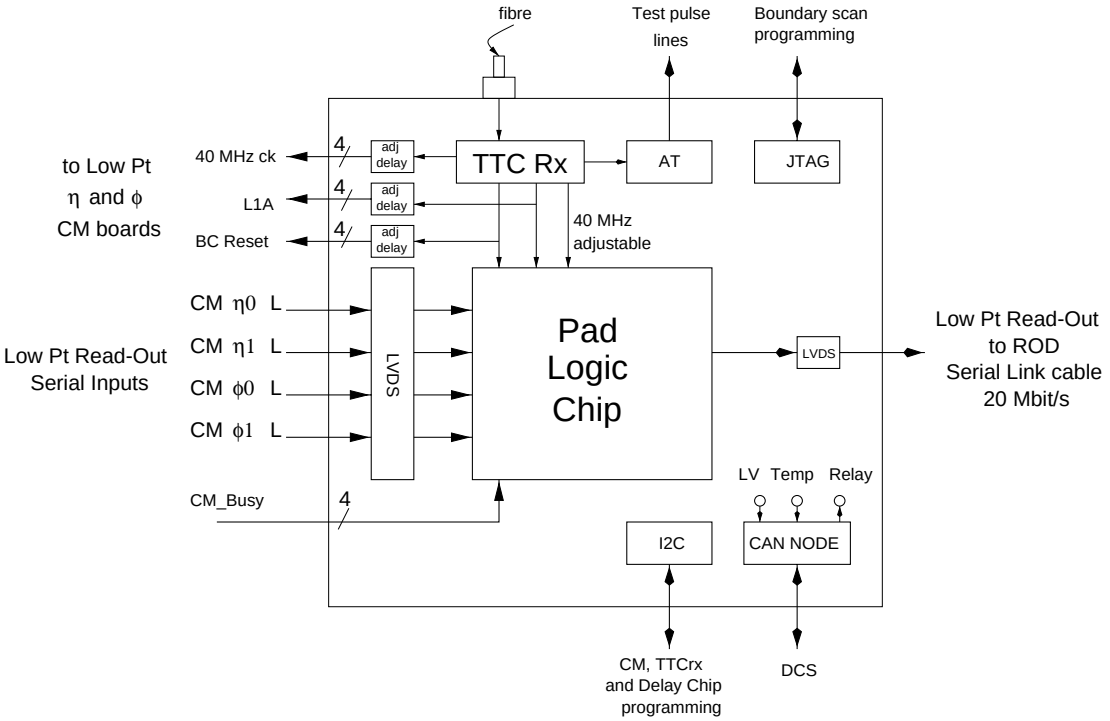

Figure 11-12 Block diagram of the low-p_T Pad board.

CM boards. The output read-out data are sent to the ROD via serial copper cable, asynchronously at 20 Mbit/s maximum data rate.

The high-p_T Pad board also takes care of receiving the trigger and timing signals and of distributing them to the four CM boards to which it is connected. Each Pad board receives the TTC signals over the standard TTC system described in Chapter 16. Details of how the trigger and timing signals are controlled and distributed are given in Section 11.1.10.

All the programming, monitoring and control functions of the board are performed through either the I2C, JTAG or the DCS and the TTC system.

11.1.6.3 High-p_T Pad board

The high-p_T Pad board combines the read-out information of two η and two ϕ high-p_T CM boards and all of the trigger information generated by the four low-p_T CM boards and the four high-p_T CM boards. A block diagram of the high-p_T Pad board is shown in Figure 11-13.

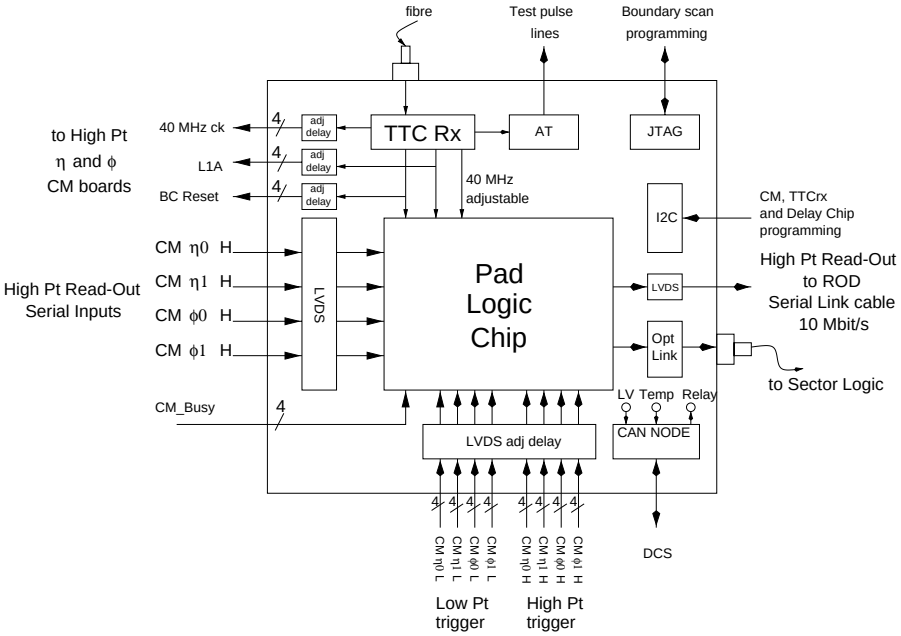

Figure 11-13 Block diagram of the High-p_T Pad board.

The read-out input data are received serially from the CM boards. The output read-out data are sent to the ROD via serial copper cable, asynchronously, at 20 Mbit/s maximum data rate. The trigger input data come in parallel from the low- and high-p_T CM boards. The 8-bit trigger pattern output is sent to the Sector Logic via an optical link, synchronously, at 320 Mbit/s. All the programming, monitoring and control functions, and timing settings of the board, are performed, as for the low-p_T pad board, through the TTC, I2C, JTAG and DCS systems.

11.1.7 Sector logic

The Sector Logic (SL) combines the trigger results for one of the 64 sectors in which the barrel trigger system is subdivided. It is located in the USA15 underground counting room at a maximum distance of 80 m (cable length) from the apparatus. Each SL board receives information from six optical links in the large sectors, and seven optical links in the small sectors. A block diagram of the SL is shown in Figure 11-14.

The logic operates in pipeline mode at 40 MHz. It receives as input seven times (six for the large sectors) an 8-bit pattern, generated by the high-p_T PL boards. In the first clock period, the logic deals with the η overlap within the sector (overlaps between different sectors are solved by the MUCTPI). In the second and third clock periods, the logic sorts the two highest-p_T muon candidates. To reduce the amount of information sent from the SL to the MUCTPI, only two muon candidates per sector are retained. In case of more than two candidates, the SL retains the two highest-p_T tracks and flags that more than two candidates were found in the sector.

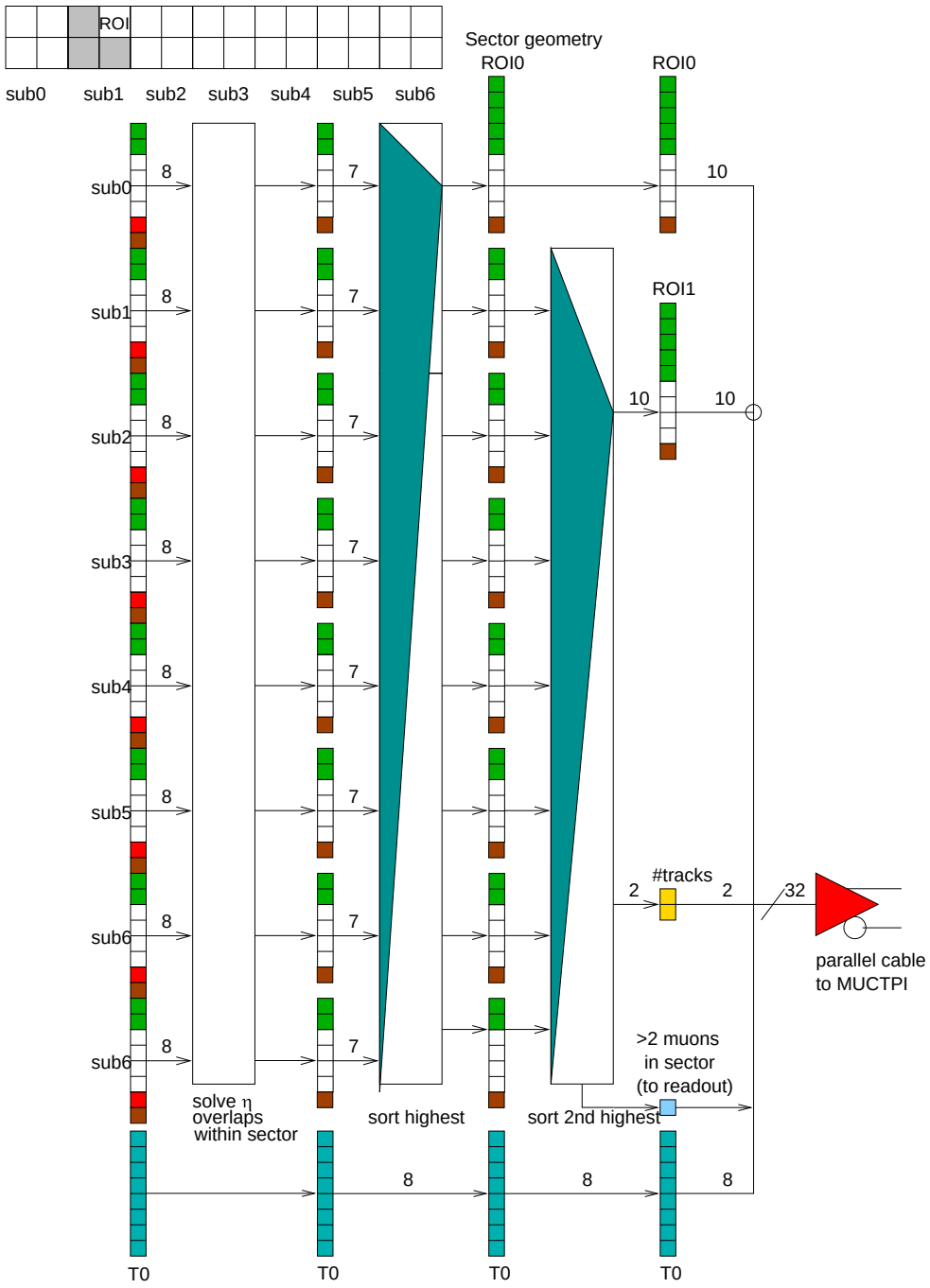

Figure 11-14 Block diagram of the Sector Logic.

As output, the SL produces a 32-bit pattern that is sent synchronously, at 40 MHz to the MUCTPI. The content of the 32-bit pattern is illustrated in Table 11-4.

The Sector Logic will be probably constructed in 9U VME standard and it will be located in USA15, very close to the MUCTPI.

Table 11-4 Sector Logic output format

Bit #	Meaning
1–5	1st candidate RoI number inside the sector
6–9	1st candidate validated p_T threshold
10	1st candidate overlap flag
11–15	2nd candidate RoI number inside the sector
16–19	2nd candidate validated p_T threshold
20	2nd candidate overlap flag
21–22	Number of triggered tracks
23–30	Bunch-crossing number
31–32	Reserved

11.1.8 Read-out scheme

The read-out of the RPC detector that is used for the level-1 muon barrel trigger is described in the ATLAS Muon Spectrometer TDR, but since a large fraction of the read-out is strongly interconnected to the trigger system, we give here, for completeness, a brief description of the read-out scheme.

The whole RPC barrel trigger system is read-out by 16 RODs. The read-out scheme is illustrated in Figure 11-15. The ROD collects the information, of both middle and outer chambers, of two half-barrel large octants. (The same scheme is also valid for the small octants, but here the number of Pads connected to the ROD is smaller.)

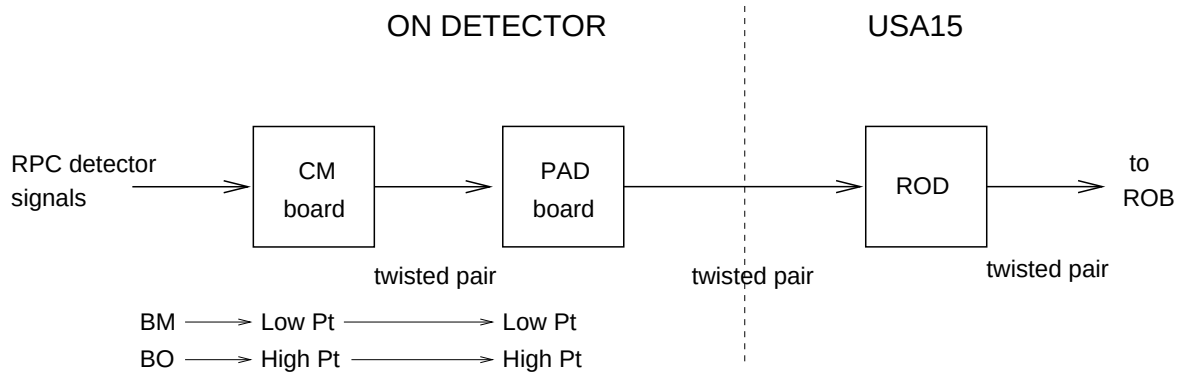

Figure 11-15 Read-out general scheme.

In the large octants, the number of Pads connected to a ROD is $6 \times 8 = 48$. In the small octants, the number of Pads is $7 \times 8 = 56$.

The connection from the Pad to the ROD is implemented through a 20 Mbit/s copper serial link, over a distance of ~ 80 m. The ROD receives the data from 56 (48 for the large octants) links, does the formatting, and sends the data to the ROB via the ATLAS standard read-out link. Figure 11-16 shows a block diagram of the ROD.

The ROD will be located in the USA15 underground counting room. A very preliminary design has been made in which the ROD is composed of four 6U VME slave modules, and one

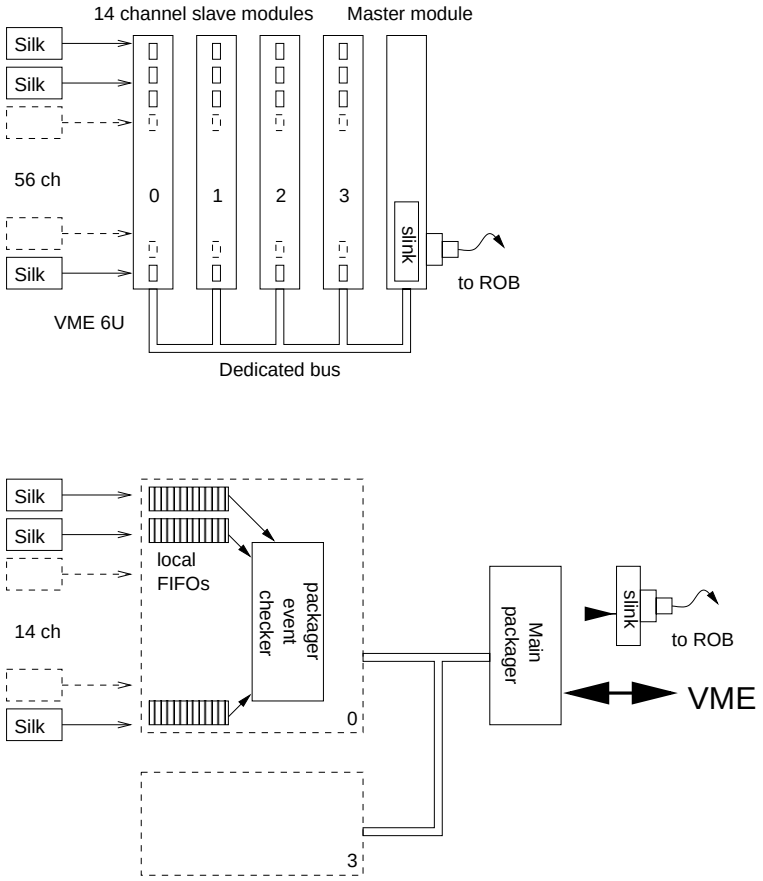

Figure 11-16 Read-Out Driver block diagram.

6U VME master module that controls the activity of the slave modules through a dedicated bus. A slave module houses 14 serial link receivers. The data of each receiver are transferred into a local FIFO from where they are moved to the master module, by a packager circuit. The master module has interfaces to the VME bus and the read-out link, that sends the data to the ROB at a maximum data rate of 1.2 Gbit / s.

11.1.9 System interconnections

The general interconnection scheme is shown in Figure 11-15 for the read-out and in Figure 11-17 for the trigger. The front-end boards are attached to the detector at the end of the RPC strip. The modularity of the front-end boards is eight channels per board. From the front-end, the RPC signals are brought to the CM boards which pass them on to the low-p_T and / or high-p_T Pad Logic boards.

From the Pad Logic boards, the trigger data are sent to the Sector Logic and then to the MUCTPI, while the read-out data are sent to the ROD.

Connection from RPC front-end to CM boards

The connection from the front-end to CM boards is implemented on twisted-pair cables; the numbers and types of cables are shown in Table 11-5.

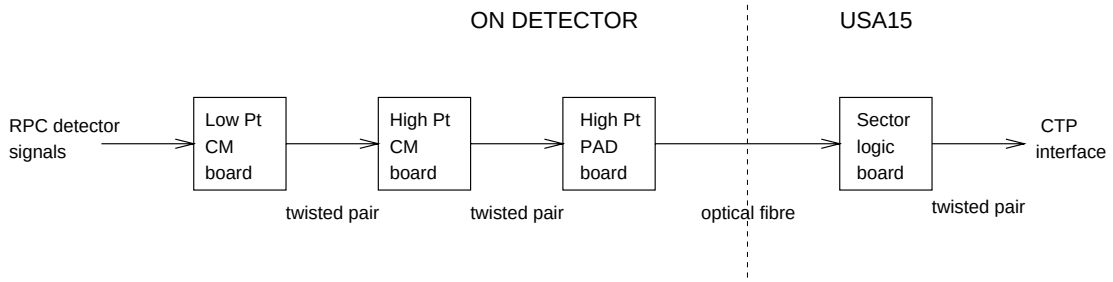

Figure 11-17 Trigger interconnection general scheme.

Table 11-5 Connection from RPC front-end to CM boards.

	Type	Length	Nº. of pairs	Nº. of cables	Signals
Low-p_T	Twisted	2 m	32	3328	IL0, IL1
Low-p_T	Twisted	2 m	48	3328	JL0, JL1
Low-p_T	Twisted	4 m	48	1664	JL0, JL1 from adjacent ϕ CMs
High-p_T	Twisted	2 m	48	3328	JH0, JH1
High-p_T	Twisted	4 m	48	1664	JH0, JH1 from adjacent ϕ CMs

Connection from CM boards to Pad boards and from low-p_T CM boards to high-p_TCM boards

The connection from CM boards to Pad boards is implemented on twisted-pair cables. The numbers and types of cables are shown in Table 11-6.

Table 11-6 Connection from CM to Pad and from low-p_T CM to high-p_T CM boards.

	Type	Length	Nº. of pairs	Nº. of cables	Signals
Low-p_T	Twisted	5 m	4	1664	Low-p_T trigger result
Low-p_T	Twisted	< 1 m	1	1664	Low-p_T serial out
Low-p_T	Twisted	5 m	32	1664	Low-p_T trigger pattern (KL)
High-p_T	Twisted	< 1 m	4	1664	High-p_T trigger result
High-p_T	Twisted	< 1 m	1	1664	High-p_T serial out

Connection from Pad board to ROD

The connection from the Pad to the ROD is implemented using a copper serial link, over a distance of ~ 80 m. The main features of the prototype link (SILK) are shown in Table 11-7.

Four differential pair lines, driving LVDS signals, are used for data, control and clock transmission. A block diagram is shown in Figure 11-18.

Table 11-7 Copper-link prototype main features

Data word size	16 bit
Transmission type	synchronous NRZ
Transmission speed	10 Mbit / s
Board clock frequency	40 MHz
Remote test capability	CCITT 0.151 0.150

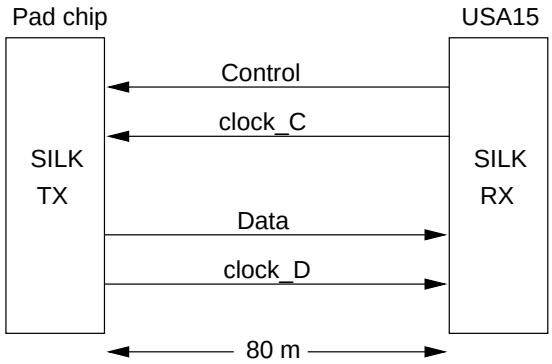

Figure 11-18 Link block diagram.

Connection from high-p_T Pad board to Sector Logic

The connection from the high-p_T Pad board to the Sector Logic is implemented using an optical link. The baseline design is based on a radiation tolerant GaAs transceiver chip developed in Rome by INFN (MATCH chip). This device works on 32-bit words, in asynchronous mode, at a maximum user bit rate of 800 Mbit/s. Table 11-8 shows the chip specifications.

Table 11-8 MATCH chip specifications

32-bit parallel word asynchronous transmission
Auto-reset at each transmitted word
Full duplex
ECL serial Manchester coded data
0.6 to 1 Gbit/s tunable frequency range
Transmission error flag
132-pin PGA package
3.5 Watt power dissipation

Figure 11-19 shows the implementation of the link. Using the MATCH chip, one 32-bit word can be sent every two bunch crossings. Data from the high-p_T pad board from two bunch crossings are packed into the 32-bit word, allowing up to 16 bits per bunch crossing. This leaves ample room to add extra information, such as error detection codes, to the 8-bit output of the PL. Note that the extra latency introduced using this scheme has no effect on the overall LVL1 latency for ATLAS since the RPC trigger result still arrives considerably earlier than those from some other parts of the trigger. Nevertheless, alternatives to the MATCH chip will be considered if they meet the requirements.

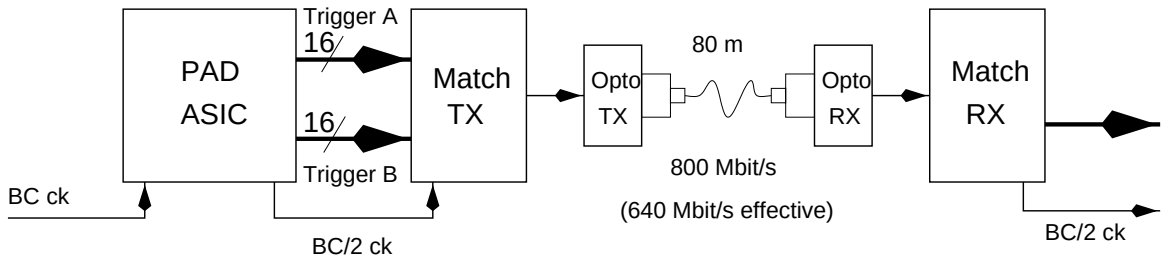

Figure 11-19 Block diagram of the optical link from high-p_T Pad to Sector Logic.

Connection from Sector Logic to the MUCTPI

The Sector Logic output is a 32-bit pattern, synchronous at 40 MHz with the machine clock. Since the SL is located in USA15 very close to the MUCTPI, this connection is implemented on a 32-pair twisted cable carrying differential ECL level signals.

11.1.10 Timing and trigger distribution

The distribution of the timing and trigger is made through the ATLAS TTC system [11-12], based on optical-fibre signal distribution as discussed in Chapter 16. The TTC system for the barrel trigger is segmented in three partitions (Table 11-9). Each partition allows independent running of parts of the trigger system for test purposes.

Table 11-9 TTC system partitioning.

Partition #1	On-detector $\eta > 0$	416 destinations	one per Pad
Partition #2	On-detector $\eta < 0$	416 destinations	one per Pad
Partition #3	USA15	80 destinations	16 RODs + 64 SL
Total		912 destinations	

The on-detector timing and trigger distribution is shown in Figure 11-20. From the TTCrx chip

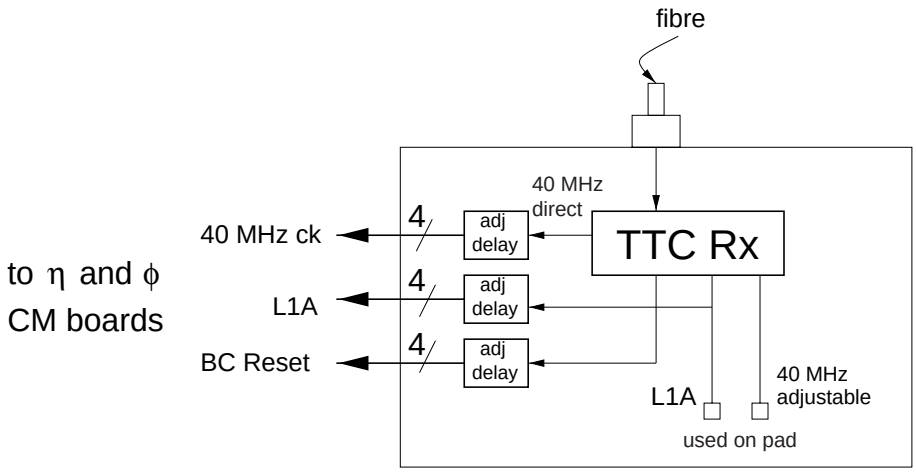

Figure 11-20 On-detector trigger and timing distribution.

mounted on each board, the L1A, BC Reset and three machine-clock signals (one direct and two with adjustable delays) are available.

The L1A signal is used inside the Pad board and it is also sent via a four-channel adjustable delay chip to the four CM boards connected to the Pad board. One of the two adjustable clock signals is used inside the Pad board, while the direct clock signal is sent to a four-channel adjustable delay chip and then to the four CM boards. Also the BC Reset signal is sent through a four-channel delay chip to the CM boards.

A test-pulse command (PPS) is also decoded from the TTCrx chip and then delayed and fanned out to eight RPC test-pulse inputs.

The use of the TTC signals and commands will be explained in Section 11.2.

11.1.11 The trigger latency

A summary of the contributions to the latency for the barrel trigger is given in Table 11-10. As discussed in Chapters 13 and 18, the trigger results from the barrel trigger arrive earlier at the MUCTPI than those of the end-cap system.

Table 11-10 Level-1 muon barrel latency (in bunch-crossings).

Muon barrel latency	BCs	Total BCs
Time-of-flight	3	3
Chamber response and shaping	1	4
Propagation inside RoI	2	6
Local processing for high- and low-p_T	6	12
Pad Logic	3	15
Connection from Pad to Sector Logic	16	31
Sector Logic processing time	5	36
Time at input to MUCTPI		36 (950 ns)

11.1.12 Environmental issues

In the design of the board trigger system two major environmental problems in the ATLAS experimental cavern have to be faced: damage of the electronics due to radiation and the presence of a high magnetic field. Although the radiation level in the muon spectrometer is less than in other parts of the ATLAS apparatus, the problem of radiation damage has to be addressed. Also, the magnetic field problem cannot be neglected since it could impose some constraints on the location of the electronics.

11.1.12.1 Radiation tolerance

The radiation dose accumulated on the muon spectrometer over ten years of running is indicated in Table 11-11. To limit the problem of radiation damage of the electronics, the first fundamental rule is to reduce, as much as possible, the amount of electronics located in the cavern. A large effort has therefore been made to locate the Sector Logic electronics in USA15. This has increased the number and length of links, but has partially solved the radiation-damage problem.

Table 11-11 Radiation doses accumulated in 10 years of running in the muon spectrometer (worst location).

Neutron radiation	$\sim 6.8 \times 10^{11}$ cm^{-2}
Gamma radiation	~ 5.6 Gy

For a safe operation of the rest of the electronics, located in the cavern, commercial components must be avoided and intensive use must be made of dedicated radiation-tolerant ASICs. As many functions as possible are implemented in such ASICs. Any commercial components to be used in the cavern will be qualified for radiation tolerance.

Concerning the use of radiation-tolerant processes for the design of ASICs, a choice must be made among some existing technologies [11-13]:

DMILL DMILL is a process developed in the framework of the RD–29 project. Its radiation tolerance is well proven for large radiation doses. The process is less dense than other standard processes and the software tool for designing chips still needs to be improved.

GaAs The radiation tolerance of the GaAs process seems to be proven, although some confirmation must still come from measurements. This semiconductor is more expensive than silicon, and the software tools for the design are relatively poor.

Deep submicron CMOS (< 0.5 μm) From preliminary and very encouraging results of the RD–49 project, deep submicron processes seem to be sufficiently radiation tolerant for the radiation level of the muon spectrometer. These processes are commonly available commercially and the software tools are well developed. This could be an acceptable solution for a large fraction of our on-detector electronics (although the development price is rather high). In Table 11-12 some relevant parameters for deep submicron CMOS processes are presented.

Table 11-12 Deep submicron CMOS main radiation-tolerance parameters

Gamma dose	~ 200 krad
Gamma dose with enclosed geometry	~ 10 Mrad
V_T shift	< 10 mV for any dose
Neutron degradation	8% g_m loss @ 10^{14} n cm^{-2}

In the barrel trigger design two kinds of on-detector boards are used: the CM board and the PL board. The main element of the CM board is the CM chip, that will perform almost all the functions of the board. This chip will be developed in 0.25μm CMOS technology. The main element of the PL board is the Pad Logic chip which will be developed in 0.25μm CMOS.

Concerning the rest of the components located on the boards (TTCrx, LVDS drivers and receivers, programmable delays, JTAG interface, CAN node and voltage regulators, and electro-optical converters), we plan to take advantage of the common LHC developments in these fields (some of them already existing).

For the two types of link transmitters located on the apparatus, we plan to use the GaAs MATCH chip for optical transmission of the trigger data, and to incorporate in the pad logic chip the transmitter of the copper link for the read-out data.

11.1.12.2 Magnetic field

The magnetic field can impose some constraints on the location of the electronics, although it is not a problem for on-board electronics, since the use of components sensitive to magnetic field can be avoided.

The magnetic field is a problem for the power supplies since we plan to install them in the cavern. It is thought that the existing power supplies can work well up to ~ 300 Gauss although this needs to be confirmed. However, in ATLAS, 300 Gauss magnetic field can be reached only at ~ 13 m from the interaction point, very close to the wall of the cavern.

CERN has established a working group on power supplies to solve this problem. We will follow the work of the group. At present the solution seems to be in the use of the right materials and in shielding the supplies in a proper way. The first tests are encouraging and the final results will come at the end of 1998.

11.1.13 Detector Control System

The standard ATLAS Detector Control System (DCS) is used in the barrel trigger. The system will take care of controlling and monitoring some parameters on the on-detector electronics. Each board sitting in the cavern has a voltage and temperature control and an on–off relay to switch off the board in case of need. The block diagram of the control system for the on-detector electronics is shown in Figure 11-21.

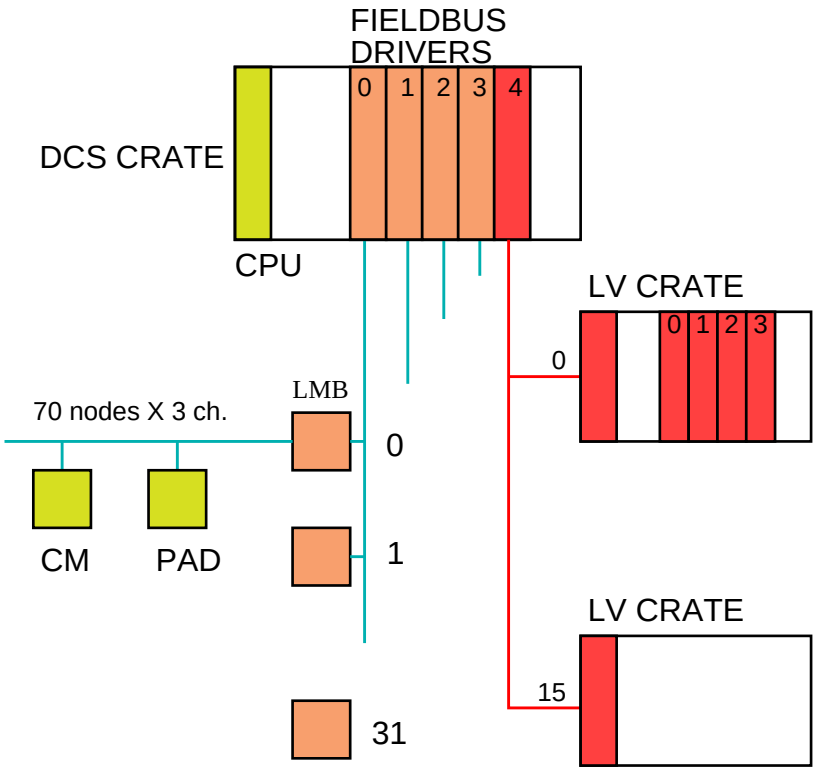

Figure 11-21 DCS block diagram.

One Local Monitor Board (LMB) is installed on the detector for each of the 64 trigger sectors. The LMB will control all the CM boards and PL boards of the sector. The total number of boards for a large (small) sector is 56+14=70 (48+14=62). For each board three DCS channels are needed: one for voltage control, one for temperature control and one for the on–off relay. The communication and control is performed via the CAN standard fieldbus. In total, 12672 DCS channels are required for the whole barrel trigger.

The LMBs are connected to fieldbus driver modules. In total, four fieldbus drivers are needed, since each module can control up to 16 LMBs. The fieldbus drivers are housed in a crate located in the USA15 counting room. This crate also contains a CPU and an additional fieldbus driver to control the Low Voltage system that, in case of need, can be switched off for a complete sector (see Section 11.1.14 below).

11.1.14 Low-voltage system

The issues of power distribution and power dissipation are important in the design of our system. The barrel trigger electronics is distributed over a large area (thousands of square metres). Since it is not allowed to dissipate a large amount of power in the ATLAS cavern, the system should be cooled. But cooling an electronic system spread over such a large area is a relevant problem. Air cooling is not allowed, because this could have some impact on the precision performances of the MDTs. The only solution would be a liquid cooling, but this implies the construction of a long and complex cooling pipe distribution system, and the circulation of a large amount of cooling liquid.

The approach that is taken, is to make a big effort to reduce the power dissipation of the on-detector electronics at a level that could be tolerated without cooling.

A very preliminary estimation of the power dissipated on the on-detector electronics has given a total of 28 kW. This value came from 30 mW / ch for the front-end and 40 mW / ch for the logic, for a total of 400000 channels. Now, after the introduction of some modification in the trigger design, this power dissipation will be reduced. A number of design decisions have been made that minimize the power dissipation: the use of LVDS signal instead of the ECL to transmit the signals from the front-end to the trigger logic, and the intensive use of deep submicron CMOS chips, powered with 3.3V or less, in which we implement almost all the function required by one board. It is clear that the final power consumption will only come when the final detailed design of every part of the apparatus is ready. However, it can already safely be said that the power dissipation will be < 20 mW / ch for the front-end and < 30 mW / ch for the trigger logic. Based on that, we have estimated the power consumption of the different parts of the apparatus illustrated in Table 11-13.

Table 11-13 Power consumption of the barrel level-1 muon trigger

Front-end channel	20 mW / ch
Trigger-logic channel	30 mW / ch
CM board	2.5 W / board
PL board	2.5 W / board
Front-end sector	120 W / sector
Trigger-logic sector	180 W / sector
Global dissipation	19.2 kW

The power distribution follows the segmentation of one power supply per sector. In total we will have 64 power supplies, located in 16 crates around the detector at $\eta = 0$. Each low voltage crate is controlled by means of the DCS system based on the use of the standard CAN fieldbus. Figure 11-21 shows how the low-voltage system is controlled. Each low-voltage crate has an interface connected to a fieldbus driver housed in the DCS crate, located in the USA15 counting room.

Table 11-14 Low-voltage specifications

Type	switching
Max power	300 W
Regulation	± 0.15%
Noise and ripple	< 10 mV pp, 0–40 MHz
Short-term stability	0.15% over 24 hours
Temperature coeff.	< 0.02% / 1°C

The trigger logic is supplied only with at least one voltage line per sector at 3.3V or less. Table 11-14 contains the most relevant specification for the trigger-logic low-voltage supplies.

11.1.15 Grounding and shielding

The grounding and shielding scheme of the level-1 muon barrel trigger follows some ATLAS ‘golden’ rules. The RPC system is isolated from the MTD system and from the support and mounting structure. The RPC chambers and the trigger electronics are contained in separated Faraday cages. The grounds of Faraday cages are connected together in groups by the same ground cable (one per sector, 64 in total), that is connected to ground in the USA15 counting room.

All the signals that penetrate the Faraday cage are in LVDS standard or optical. The cage is penetrated only by:

- LV power lines
- I2C lines
- DCS lines (CAN bus lines)
- JTAG lines
- TTC optical input
- LVDS trigger I/Os
- LVDS read-out I/Os
- LVDS PPS lines

Low-Voltage supplies are floating. In the present design, the low voltage is regulated down to the required value on each board. However the possibility to send the voltage already regulated and to monitor it through the DCS is being considered (this eliminates the power loss on the voltage regulator).

The system should provide some kind of ‘ground fault’ warning device, to monitor ground problems.

11.2 Software implementation of the system

In the preceding sections the hardware composition of the level-1 barrel trigger was illustrated, showing the different parts and their functionalities. This section illustrates how the different parts work together in a coherent way, how they interact with each other, how they are controlled, calibrated and monitored, and how test and diagnosis of the different parts of the apparatus are done: In other words it will describe what is called software implementation of the system [11-14][11-15].

The general strategy for the software implementation of the system follows some ATLAS implementation rules and some subdetector-specific ones [11-16]. There are some functions that in ATLAS should be performed in a standard way for all subsystems. Data are read out through the ROD–ROB chain, timing of the apparatus through the TTC system, and use of the standard DCS system for detector control. The other implementation rules are specific to each subsystem.

11.2.1 Data read-out

The barrel has an eight octant (0–7) azimuthal segmentation; each octant is further subdivided in two parts, covered by Barrel Large (BL) and Barrel Small (BS) units respectively; each of the two units is again subdivided in two sectors, covered by RPC chambers. We therefore have a total of four sectors (0–3) per half-barrel octant (see Figure 11-22).

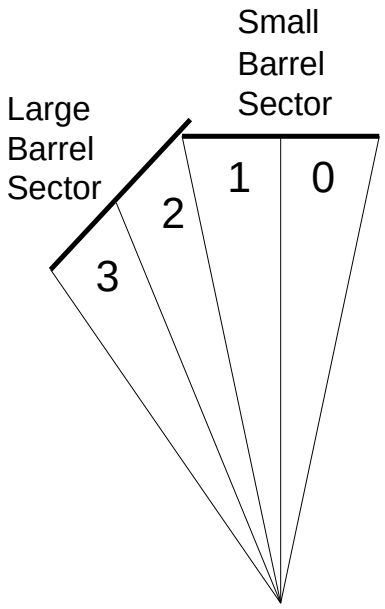

Figure 11-22 Azimuthal view of one half-barrel octant of the trigger segmentation.

The elementary hardware cell, from the read-out point of view is the Coincidence-matrix (CM). The strips of both the η and ϕ views of the RPC chambers are connected to CMs. Four CMs (two in η, two in ϕ) form the low- or high-p_T Pad. The superposition of one η CM and one ϕ CM within a Pad gives a RoI of size $\Delta\eta \times \Delta\phi = 0.1 \times 0.1$. The low-$p_T$ Pad performs the data read-out of the trigger chambers (RPC) in the middle station while the high-p_T one performs the data read out of the outer station.

Figure 11-23 and Figure 11-24 show the RPC chamber partitioning in Large and Small sectors for a half-barrel, including the mapping of the Pads and RoIs. Read-out data from both projections for a given Pad are sent through the same point-to-point copper link to the ROD as shown in Figure 11-25. One ROD combines data from 48 Pads, combining both half-barrels and all the trigger stations for the Large Chambers: another ROD does the same for the 56 Pads of the small chambers. This gives two RODs per octant, that is 16 RODs in total (Figure 11-26); the RODs are located in USA15 and each of them is connected to one ROB, sitting in the DAQ crate.

The RPC read-out is closely connected to the Monitored Drift Tubes (MDT) read-out organization and is based on the assumption that the RPC and MDT data from the same projective area have to be put in the same DAQ crate. This allows local pre-processing in the LVL2 trigger using both RPC and MDT data, the RPC data being used to guide a track search in the MDT.

The choice of the data to be sent to the read-out must allow the following tasks: monitoring of the functioning of the hardware processor, by reproducing the level-1 trigger algorithm with a software program and the same input data; provision of information in a form that gives fast guidance to the level-2 algorithm; compliance with the standard ROB input data format.

The data format is organized according to the hardware structure: CM, Pad and ROD. Zero suppression will be applied at the level of CMs and Pads. An empty structure will not be suppressed to ensure event synchronization at every level, but it will not be propagated along the read-out hierarchy. A further level of zero suppression will be applied within a chamber pattern, keeping only the addresses of the firing strips (this applies to both the input and the output data of each CM). A CM will be read out even if it did not give any trigger.

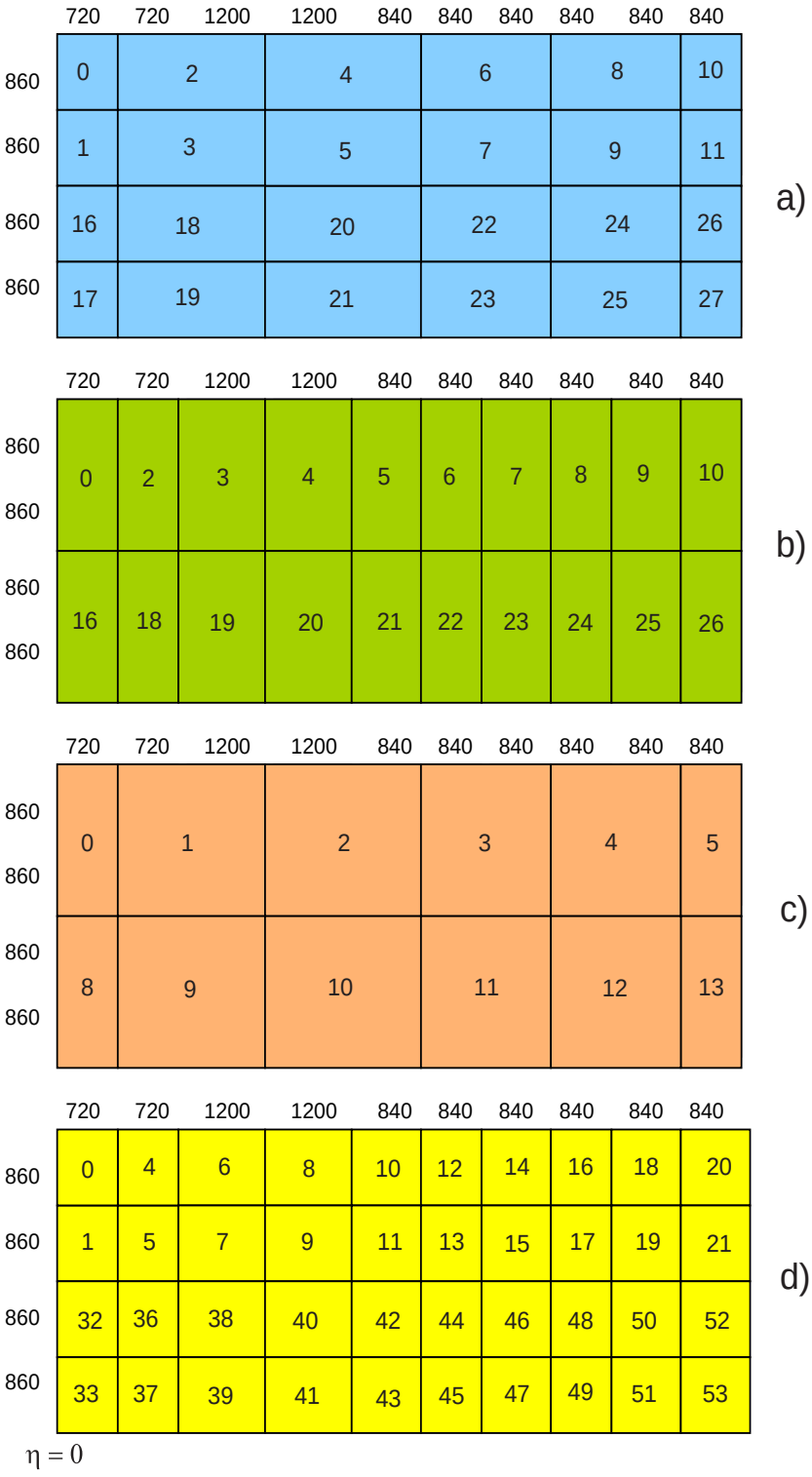

Figure 11-23 Partitioning and numbering conventions of a Large Sector: (a) ϕ strip and CM partitioning, (b) η strip and CM partitioning, (c) Pad partitioning, and (d) RoI partitioning. Chamber dimensions in the RPC1 station are indicated (in mm).

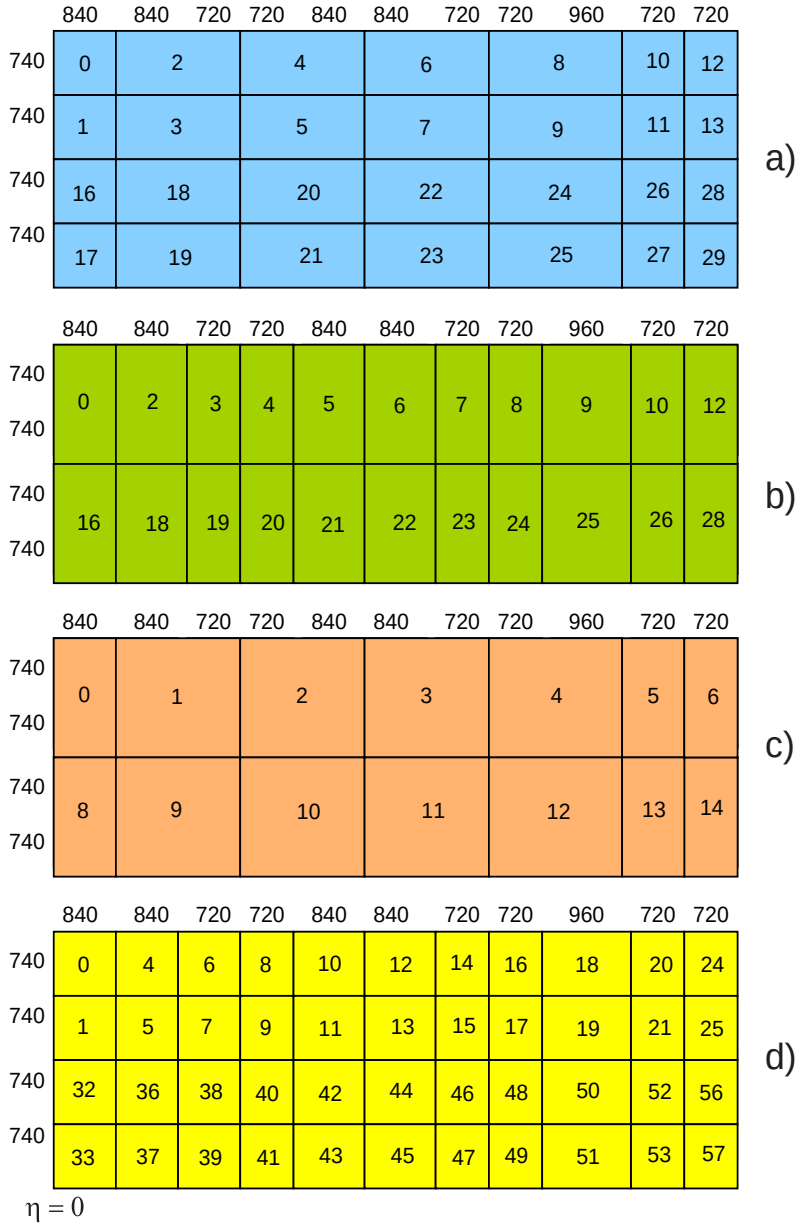

Figure 11-24 Partitioning of a Small Sector: (a) ϕ strip and CM partitioning, (b) η strip and CM partitioning, (c) Pad partitioning, and (d) RoI partitioning. Chamber dimensions in the RPC1 station are indicated (in mm).

Figure 11-27 shows the contents of the CM input and output patterns. For the low-p_T trigger, one input pattern is the 32-strip I0 plus the 32-strip I1 of the first RPC doublet. The second input is the 48-strip J0 plus the 48-strip J1 of the second RPC doublet. Low_out is the 32-bit pattern produced by the low-p_T CM plus eight more bits for local flags and thresholds information. For the high-p_T CM the first input pattern is the 32-strip I0H from the low-p_T CM output, while the second input pattern is the 48-strip J0H and the 48-strip J1H of the third RPC doublet. High_out is made of a 32-bit pattern plus eight bits of matrix information.

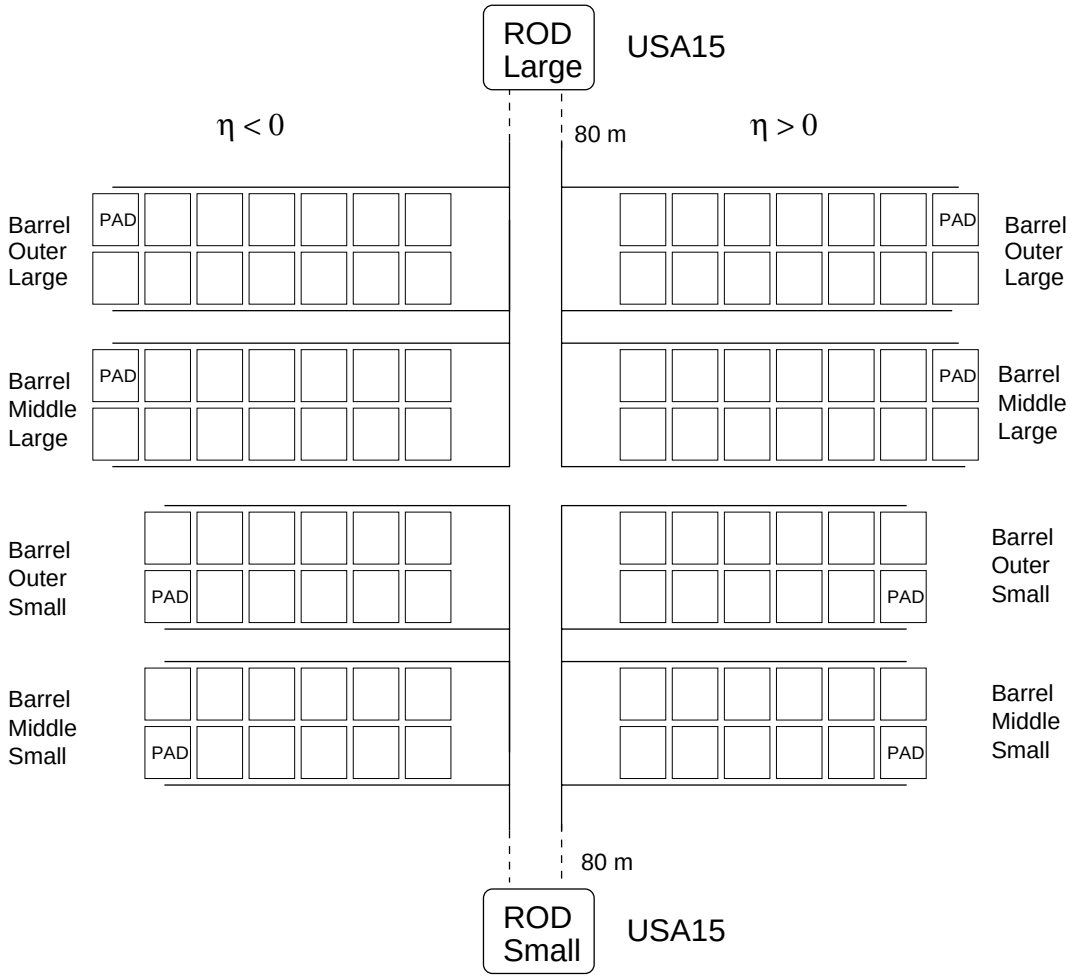

Figure 11-25 Read-out organization for RPC chambers.

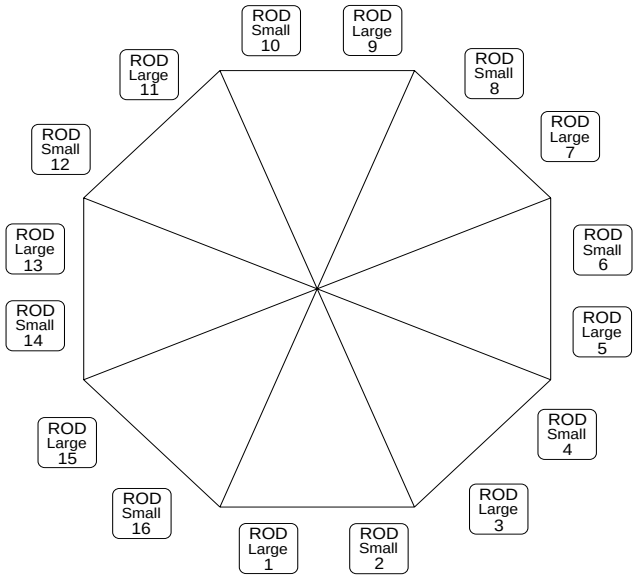

Figure 11-26 Read-Out Drivers of the RPC chambers. RPC ROD numbering follows the muon barrel layout numbering. RODs are physically located in USA15.

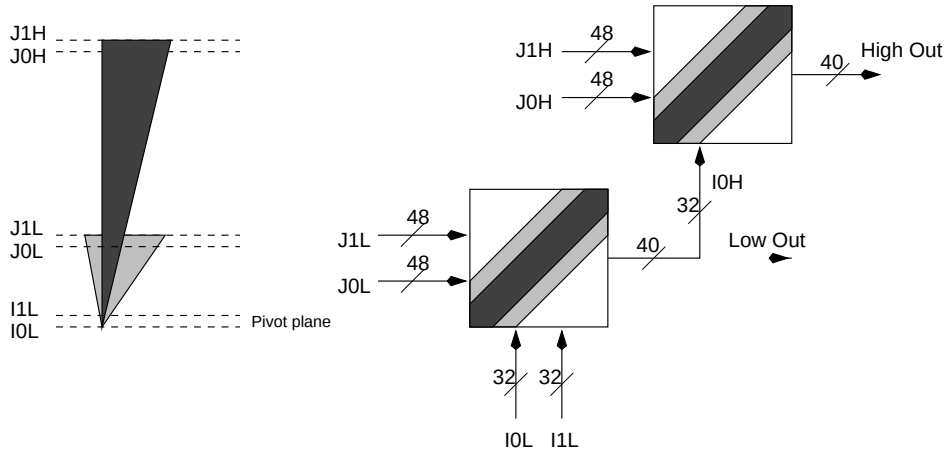

Figure 11-27 Coincidence-matrix input and output pattern.

For each CM matrix, on average 16 bytes are produced in the case of a low-p_T track candidate. Four clusters from the RPC1 and RPC2 doublets are expected. Assuming an average cluster size of 1.5 strips this accounts for six hits (12 bytes). The trigger output produces one hit (two bytes for the output pattern) and two bytes for the trigger threshold / overlap output.

Table 11-15 Read-out identifiers and numbering

ROD number	0–15	4 bit
SL number	0–63	6 bit
Pad number	0–55	6 bit
CM number	0–3	2 bit

In case of a high-p_T track 10 bytes have to be added to the previous low-p_T 16 bytes. These 10 bytes come from two clusters of the RPC3 doublets (six bytes accounting for the cluster size) and four bytes of the high-p_T trigger output.

In Table 11-15 the general read-out identifiers and numbering are shown.

As shown in Figure 11-28, each hit RPC strip will be encoded in two bytes, including the strip number and the time-interpolator measurement. In the same figure the overall event structure is shown, valid for both the CM-to-Pad link and the copper link going to the ROD. The header information is kept at minimum in order to minimize the data overhead in view of the low RPC occupancy.

Some extra information [Front-End-Bunch-Crossing Identifier (FEBCID, BCID), Front-End Level-1 Identifier (FEL1ID, L1ID)] is inserted at each level of the structure for synchronization checks. Structure identifiers, such as ROD number, SL number, etc. are generated in the hardware.

The CMs are not the only sources of read-out data. Each Pad produces data useful for monitoring the trigger system; Pad trigger patterns are sent via the copper link along with the CM data. Each SL produces, every bunch-crossing, a 32-bit trigger pattern whose content is illustrated in Table 11-4. Sixty-four such bit patterns are sent from the barrel trigger system to the MUCTPI through the fast synchronous 40 MHz trigger path. Each SL will also send read-out data, in order to be able to successfully monitor the trigger operation, through a dedicated copper link, to a corresponding SL ROD. In Figure 11-29 the ROD output data format is shown. It follows closely the required standard ATLAS event format for the I / O LDAQ modules.

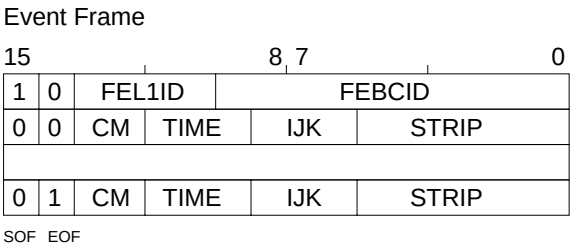

Figure 11-28 CM-to-Pad and copper-link data format.

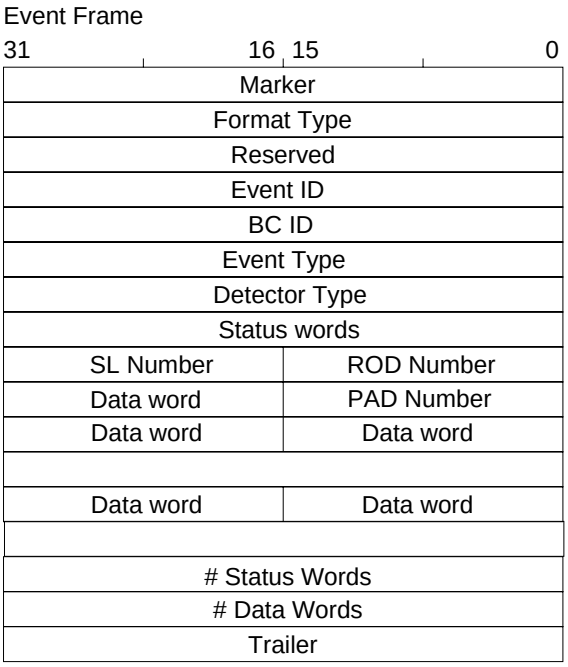

Figure 11-29 ROD data format.

11.2.1.1 Data-throughput calculation

A preliminary study on the data bandwidth requirements has been done using background calculations for the particle rates in the chamber. The input values used are shown in Table 11-16. The particle fluxes shown above give a total incoherent background flux of $10.3\,\mathrm{Hz/cm^2}$, and a coherent background of $0.7\,\mathrm{Hz/cm^2}$ (Incoherent background includes all the background sources that generate random clusters in the CMs, while the coherent background is defined as the one that generates correlated hits in the RPC doublets.)

Table 11-16 Background particle flux and RPC sensitivities used in the bandwidth calculation.

Particle type	Flux (kHz cm^{-2})	Sensitivity
e^+ e^-	2.3×10^{-3}	1
Charged hadrons	9.5×10^{-4}	1
μ	10^{-3}	1
γ	1.2	5.33×10^{-3}
n	3.3	10^{-4}

Table 11-17 shows a comparison of the bandwidth requirements. The calculations assume a safety factor of 10, to take into account uncertainties in the expected fluxes, a typical strip area of $360\,\mathrm{cm^2}$, an average cluster size of 1.5 hits, a trigger rate of 100 kHz and an encoding of hits in 16-bit words, in three cases:

- data encoding with no headers sent along the read-out path;
- data encoding with CM, PAD and ROD headers propagated along the read-out chain;
- no data encoding.

A read-out structure is assumed, where all components send data along their corresponding links in parallel, as foreseen in the final system. The final data-encoding scheme will require a data throughput which is between these two extreme cases. The data bandwidth that would be

Table 11-17 Average required bandwidths on CM, Pad and ROD links.

	Link bandwidth	Average bandwidth (16-bit encoding and no header)	Average bandwidth (16-bit encoding and full headers)	Average bandwidth (no encoding)
CM to Pad	10 Mbit / s	1.4 Mbit / s	3.0 Mbit / s	480 Mbit / s
Pad to ROD	20 Mbit / s	5.7 Mbit / s	13.7 Mbit / s	1920 Mbit / s
ROD to ROB	1 Gbit / s	0.30 Gbit / s	0.73 Gbit / s	100 Gbit / s

required, without hit encoding, is also shown. (24 time slices, corresponding to three consecutive bunch crossings, have to be transferred per strip each event.)

The current design seems adequate, but an accurate simulation of the system is necessary and will be made.

11.2.2 Control and monitoring

All control and monitoring functions of the trigger system are performed through five hardware parts: the read-out system, the Timing, Trigger and Control system (TTC), the I2C interface, the JTAG interface and the Detector Control System (DCS).

The read-out system is used for monitoring and checking data during data-taking runs, calibration runs and test and diagnosis operations. Data generated by the trigger system during data taking runs can be monitored by the run control system. Monitoring at the ROD level will be needed to allow independent running from DAQ. The main monitoring and control functions to be performed are outlined below:

- Input data quality: Hit maps are needed to check the working conditions of the trigger chambers.
- Online checks of the trigger algorithm are done using raw data and trigger data, comparing the results from processing in the LVL1 hardware with those from a software model.
- Monitoring of trigger rates, histogram filling, per sector.
- Monitoring of nearly full flags from the derandomizers has to be done to react and introduce dead time.
- Monitoring of ROB-BUSY signals, to force the level-1 CTP to introduce dead time when necessary, is needed.
- A test mode, where fake events are produced with known data, is foreseen to be able to test the read-out chain from the ROD or possibly from the derandomizers up to the ROB.
- Error-recovery procedures are foreseen, since the DAQ must not stop if a single failure is present in the read-out chain of a subdetector.

Calibration runs are used for timing calibration and momentum calibration. In both cases the appropriate set up of the trigger system parameters is made through the TTC, I2C and JTAG systems, and the data are read through the read-out system.

The TTC system performs the important functions of distributing the machine clock and level-1 accept signals and of setting up the right timing of the trigger system for different operations. A standard receiver chip, the TTCrx, is used on the detector to receive and decode the TTC signals. This chip is programmed through the use of the I2C standard fieldbus.

The functions of loading the appropriate parameters for different kinds of operations, and for test and diagnosis of the on-detector electronics, are performed through the JTAG or the I2C interface. These interfaces are part of all on-detector boards and are connected to the control system that is located in underground counting room. Since, in the present design, every on-detector electronics board is accessed by three buses (I2C, JTAG and DCS/CAN), to reduce the number of buses, the possibility of using the I2C bus and discarding the JTAG bus is being investigated.

The DCS system is used to monitor the voltage and the temperature of each board of the on-detector electronics and, if necessary, to switch off the board. It makes use of the standard CAN fieldbus system.

11.2.3 System initialization

The initialization procedure is accomplished by loading the on-detector electronics, the Sector Logic and the RODs with the appropriate parameters. The hardware used for the initialization are the TTC and the I2C and JTAG interfaces for the on-detector electronics and the VME control system for the Sector Logic and the ROD. Calibration data should be taken in order to properly initialize some of the trigger parameters. The initialization includes the following phases:

- Set the on-detector TTC circuits and the programmable delays between the TTC system clock and the coincidence-matrix, the Pad Logic and front-end boards.
- Set chamber front-end electronics thresholds.
- Set the mask-off pattern for channels that have been found noisy during previous monitoring of chambers.
- Initialize multiple trigger coincidence-matrix roads, to set up to six different p_{T} thresholds.
- Initialize coincidence-matrix input pipeline depths, one value per front-end signal cable (used to time align all input channels).
- Initialize coincidence-matrices mode registers. The mode registers are used to define the coincidence-matrix chip functionalities: low- or high-p_{T} algorithm data processing, run initialize mode, etc.
- Initialize the coincidence-matrix output pipeline depths (used to synchronize the various coincidence-matrices belonging to the same Sector Logic).
- Program digital shaping of coincidence-matrix chip inputs and outputs (used to optimize bunch-crossing identification efficiency and background rejection).
- Initialize Sector Logic input pipeline depths, to synchronize the Pad Logic belonging to the same sector.
- Initialize the Sector Logic look-up tables (used during local merging of muon candidates found in the RoIs defined in the bending and non-bending plane).

- Initialize overlap window sizes between adjacent sectors and between barrel and end-cap regions. (They are optimized to balance rejection to false dimuon triggers and to maximize dimuon trigger efficiency.)
- Set the mask for masking-off hot RoIs.

11.2.4 System calibration

Two kinds of calibration are foreseen: timing calibration and momentum calibration. The timing calibration establishes the correct set up of the timing system for beam data-taking runs, cosmic-ray runs, and test and calibration runs. The momentum calibration determines the correct set up of the of the p_T thresholds of the trigger system.

11.2.4.1 Timing calibration

Strategy for setting up timing with beam

In the following timing calibration strategies a coarse time alignment, using TTC and RPC cable propagation delay measurements, time-of-flight calculations and detector response is performed before starting the timing procedure.

Two different strategies are required, one for the local synchronization of front-end signals coming from different stations within a trigger tower (Pad), the other for the global synchronization of the trigger system.

Local time calibration: The front-end signals from the three stations enter the CMs with different delays due to time-of-flight, propagation along strips and cable length. Each CM can realign the input data using the programmable-depth input pipelines, which act independently per octet of discriminator signals.

Before calibration the input pipelines will be set to zero delay. In Figure 11-30, an example of the timing of signals before calibration is shown.

The CM processing is driven by a 320MHz clock, derived from the 40MHz BC clock coming from the TTCrx chip mounted on each Pad. In this way each bunch-crossing period is subdivided into eight time slices, and both front-end and trigger outputs are assigned to a time slice via the 3-bit time interpolator circuit. This facility will be used for monitoring both the detector and the trigger system.

The RPC front-end discriminator has a fixed shaping time of around 10ns. An edge detector will sample this signal at the input of the processor pipeline.

The time-slice information will be sent into the level-1 read-out pipeline, while a shaped output will go to the coincidence-matrix. Before calibration the shaping time of the input signals to the CM will be set to the maximum, eight time slices, to be able to identify muon candidates effectively even if the timing is not precisely set.

The same calibration procedure is applied to the two I and J doublets.

The matrix output will assign the muon candidate to a specific bunch crossing, but the detector and trigger data belonging to a muon track will be spread on a number of bunch crossings.

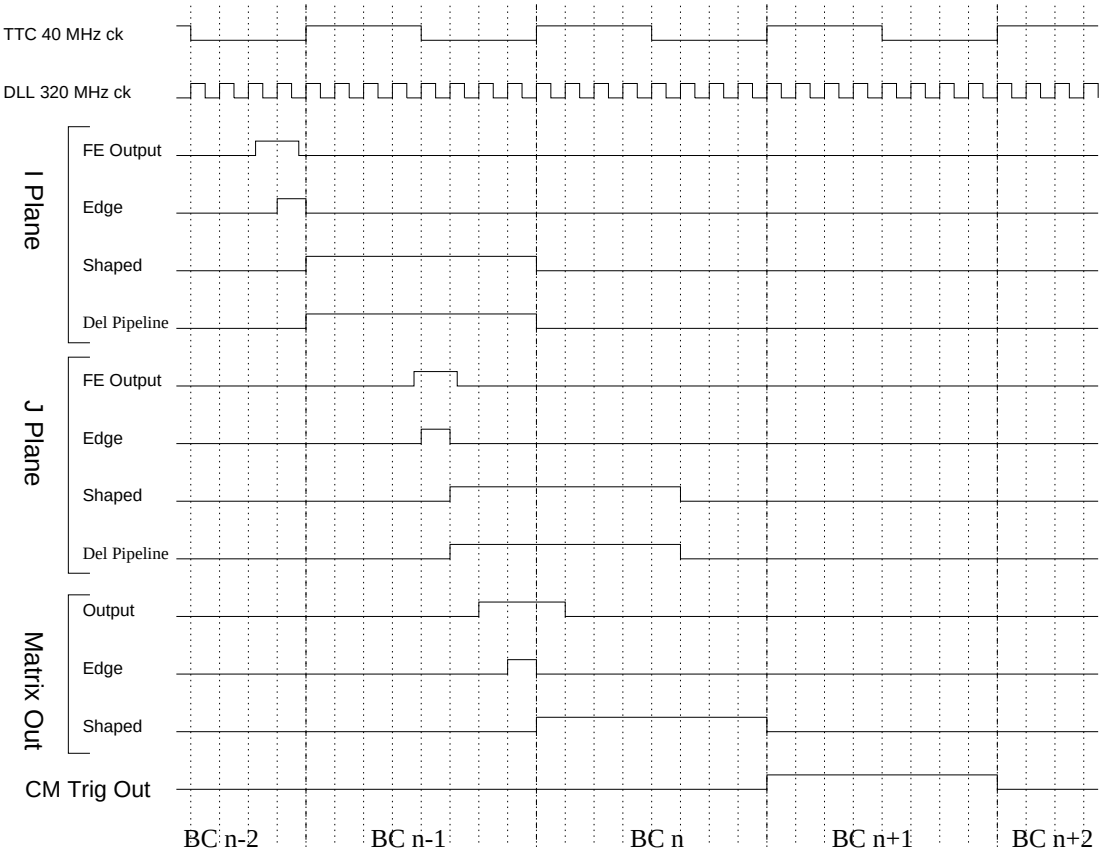

Figure 11-30 Timing of local processor signals before calibration.

For this reason the read-out part of the CM is able to send data belonging to up to five bunch crossings around the triggered one.

It will be possible to run uncalibrated with a single-muon level-1 trigger at the expense of a lower rejection to fake tracks and higher required read-out bandwidth.

An analysis of the data collected with this trigger will allow suitable delays to be determined that can then be programmed into the variable-depth input pipelines of the CMs, establishing temporal alignment of the different inputs. An example of the timing of signals after local calibration is shown in Figure 11-31.

Once the input delays have been correctly set up, the shaping time of the I and J signals can be shortened, reducing the rate of fake triggers from accidental coincidences. The shaping times will be set to the minimum values that give efficient track finding, taking into account the spread of signal arrival times due to variable time-of-flight, the detector resolution of 1.5 ns, the range of signal propagation times, the discriminator walk and the quantization error.

Final adjustment to be made are to adjust the clock phase from the TTCRx to its optimal value and to set the shaping of the CM output to match the 40 MHz external operation. This fine tuning is done by monitoring the CM trigger output, time tagged with a 3.1 ns least significant bit precision. The TTCRx phase must be adjusted to centre the time distribution inside the 25 ns bunch-crossing interval.

Since hits belonging to a muon track will belong to a combination of four out of eight CMs of a low- and high-p_T Pad, this operation will align in time locally the low- and high-p_T parts, and the bending and non-bending coordinates.

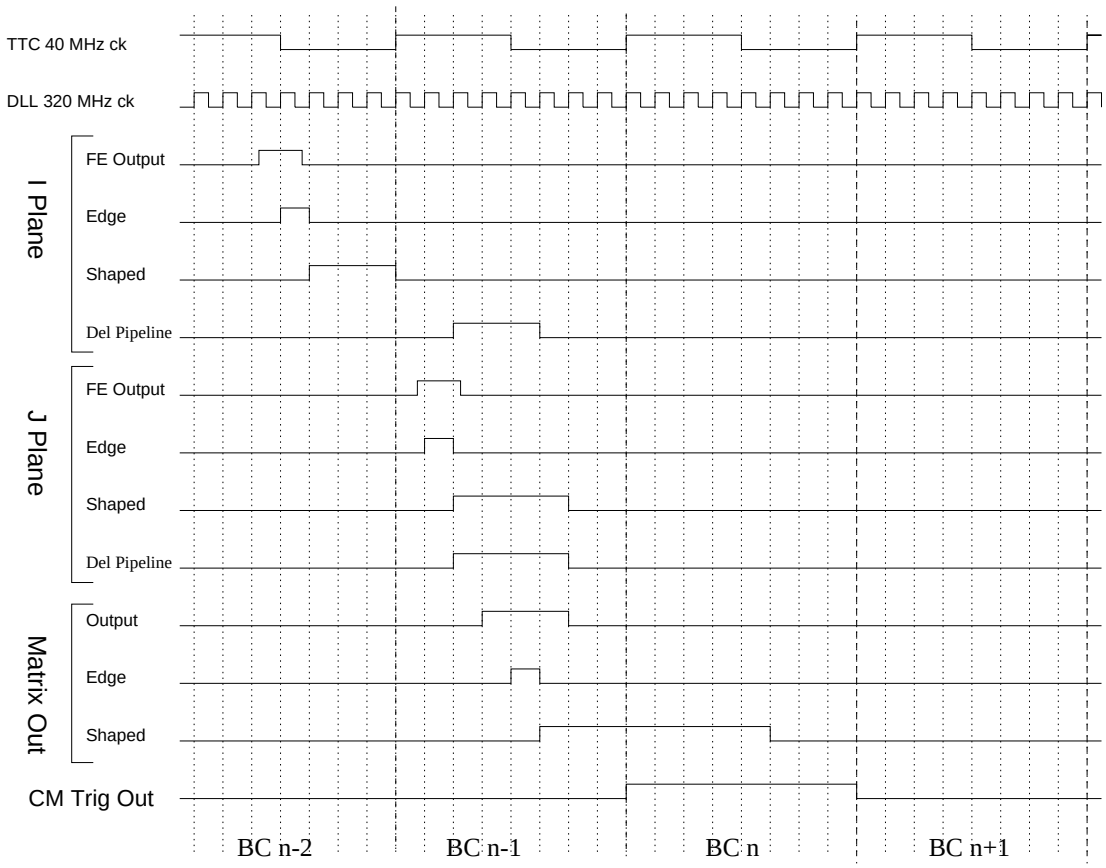

Figure 11-31 Timing of local processor signals after calibration.

This scheme has a powerful monitoring capability, because the CM inputs and outputs are sent to the read-out, time measured with a precision of 3.1ns least significant bit, which is much finer than the bunch-crossing interval of 25ns.

The monitoring needs of the detector system are also met.

Global time calibration: After the local time-calibration procedure described above, the different inputs and circuits within each pad will be correctly timed-in relative to each other. However, the timing calibration between the different pads, sectors and the rest of the LVL1 system still have to be adjusted.

The global synchronization procedure will first look for two muon candidates, triggering on single muons, and searching for a secondary muon trigger in the five BCs range around the triggered BC. The secondary muon can come from the same track that has been seen twice because of bad synchronization among different parts of the apparatus (low- and high-p_T CMs, overlap between Pads, overlap between Sectors, overlap between barrel and end-cap) or from an additional real muon belonging to the same event. The fake secondary muon can be easily recognized.

The relative phases of the TTCrx are then adjusted acting on the phase of the 40 MHz clock, until all muon tracks will assigned to the same BCID, either collapsing on a single muon track or generating a dimuon trigger.

Strategy for setting up timing with cosmics

Rate calculations are necessary to understand which fraction of the spectrometer can be calibrated with cosmics. The $\cos^2\theta/E^2$ dependence and the effect of the access pits have to be studied. Timing settings will be different for beam and for cosmics and a different calibration scheme has to be foreseen at least for the upper part of the experiment.

Local calibration with cosmics: In the case of tracks coming from the interaction region the propagation of signals along cables follows the particle flight, while for cosmic muons signal propagation and particle flight, in the upper part of the apparatus, are in opposite directions.

It will still be possible to align signals in time to make local coincidences, but the requirements on the CM design will be increased in one or both of the following ways:

- wider range of input delays (to allow for reversing the timing in the upper part of the apparatus);
- longer shaping for coarse coincidences before calibration.

The effect on the maximum time walk of the input signals due to different cable paths and lengths has to be carefully studied before freezing the CM design. The final layout values are being calculated at the time of writing.

Global calibration with cosmics: A cosmic trigger will look for muons pointing to the interaction region and, after following the same rules for the global calibration as with beam, a cosmic muon will fire the di-muon trigger at level-1 (Figure 11-32).

The lower part of the experiment uses the beam-run timing settings, while the upper arm is offset to earlier bunch crossings.

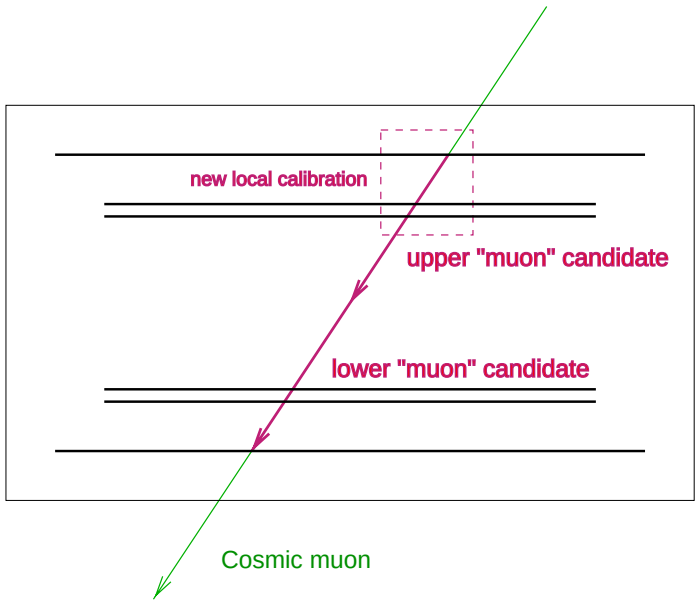

Figure 11-32 Level-1 cosmic-muon trigger.

Strategy for setting up timing in test and calibration runs

It is possible to make an initial set-up of the timing without using beam or cosmic runs. This requires a special command 'prepulse' (PPS) to be distributed by the TTC system, followed by an Level-1 Accept signal after a fixed time (see Sections 15.2.3.3 and 16.5.3).

The PPS command is received and decoded by the TTCrx circuit on the Pad board. The decoded command is transmitted to the four coincidence-matrix boards and to all front-end boards connected to the Pad. On the PPS command, the front-end boards set to 'one' the outputs of all the strips belonging to the board. The outputs of the front-end boards are connected to the inputs of the CM boards. Here the input bits of the CM chip can be masked individually to generate a trigger on a predefined pattern. The generated trigger is read-out by the Level-1 Accept signal that will follow the PPS command.

The timing settings are the same as for the beam data-taking procedure, already illustrated in the previous paragraphs. The only difference is in the time of flight that in this case does not need to be compensated since it is the same for all the trigger system.

The described procedure will also be used to test the full read-out chain, since it allows all the strips of the apparatus to be read simultaneously.

11.2.4.2 Momentum calibration

Momentum calibration is necessary for setting the p_T thresholds of the trigger system. The system must operate with three low-p_T and three high-p_T thresholds working concurrently.

At the beginning of data-taking, for each part of the apparatus, the setting of the thresholds is made by loading in the coincidence-matrix chips roads generated from the simulation programs. These roads should already be very close to the final ones. After a period of data-taking (the duration of this period has to be studied), when there is enough statistics, roads can be checked and if necessary updated by studying reconstructed muon tracks (p_T measured in the muon spectrometer and in the inner detector).

11.3 Prototype demonstrator programme

A long and intensive demonstrator programme was carried out in the last few years to demonstrate the feasibility of the barrel trigger system design [11-17]–[11-21]. The programme was dedicated to detector studies and associated electronics. The detector studies are described in Ref. [11-8]; here we report on the electronics studies for designing the level-1 muon barrel trigger processor. This part of the studies was carried out in the framework of the RD27 project [11-21].

The main goal of the demonstrator programme was to design and build, on a small scale, a trigger system that meets all the most important trigger requirements and that is conceptually very close to the final ATLAS trigger system.

The programme was mainly developed in three different phases and each phase was concluded with a series of tests and measurements, performed on a test-beam in the CERN North Area.

In the first phase a system was developed just to test the planned trigger algorithm, to implement and to demonstrate the possibility to identify the LHC machine bunch-crossing. Here the trigger processor was based on coincidence-matrix boards, connected to the RPC front-end and implemented through a series of commercial GaAs crossbar switches [11-22]. The results were very encouraging: the whole trigger system, made by the RPC and the processor electronics, performed very well the trigger algorithm and gave an excellent bunch-crossing identification capability, since the global time resolution, of the detector and of the electronics, was < 2 ns (excluding propagation delays on strips).

Based on the results of the first tests, something much closer to the final ATLAS trigger system was built, from both a detector and an electronics point of view. First a small-size trigger tower and then a full-size trigger tower were built. Both were equipped with an electronic processor based on a dedicated CM demonstrator ASIC. The systems were tested on the ATLAS H8 test-beam line.

11.3.1 The coincidence-matrix demonstrator chip

The most important building block in the design of the barrel trigger demonstrator system was the coincidence-matrix demonstrator ASIC [11-23], [11-24]. This ASIC contains, in a reduced scale, the most important functionalities that must be implemented in the level-1 barrel trigger.

The ASIC can work in fully combinatorial and fully pipelined operation or in any combination of the two. The dimension of the matrix is 8×24 and two thresholds can operate simultaneously. The chip can be programmed to implement the low- or the high-p_T algorithm. In the case of the low-p_T algorithm, a 3/4 majority coincidence of the four inputs coming from the two RPC doublets is performed. In the case of the high-p_T algorithm, a 2/3 majority coincidence of a high-p_T RPC triplet, plus the low-p_T output validation is performed. (In the previous ATLAS trigger design the high-p_T RPC station was made of a triplet instead of a doublet.) The ASIC contains the capability of adjusting the input cable delays, through a variable-length programmable input pipeline of four step length. Also, the possibility of masking noisy channels or missing planes is implemented. Figure 11-33 shows the block diagram of the ASIC.

The ASIC was implemented in a Fujitsu 0.5 micron CMOS 34K gate-array. From the tests performed on it, we have measured a maximum skew in the chip operation of 1.8 ns and a maximum pipeline working frequency of 120 MHz.

A number of 6U VME boards were made based on the ASIC (see Figure 11-34), to be used as trigger-processor elements.

The main element of each board is the coincidence-matrix ASIC, to which are connected the input signals of the RPC and the output signals of the trigger result. At the input, the signals are converted from ECL to TTL levels suitable for the 3.3V power supply of the CM. Additional input/output connections are the XIN and YIN serial inputs, and the THR0 and THR1 NIM trigger threshold outputs. A Xilinx FPGA circuit is used for the ASIC control and the VME interface.

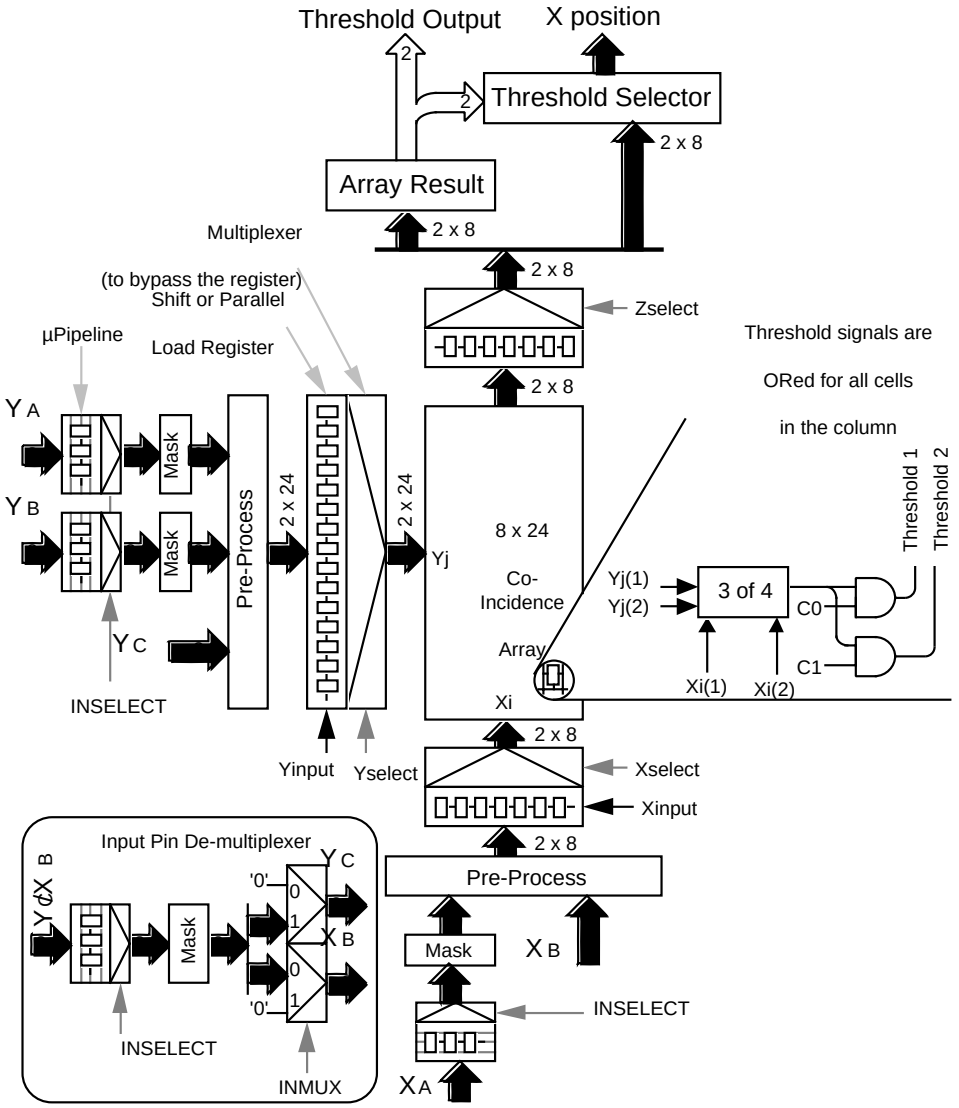

Figure 11-33 Block diagram of the coincidence-matrix demonstrator ASIC.

11.3.2 Trigger-tower demonstrator systems

Two trigger-tower demonstrator systems were built and tested in 1996 in the ATLAS H8 test-beam line [11-25]. The first demonstrator was a reduced-size trigger tower of $50 \times 50\text{cm}^2$ (Figure 11-35), composed of two RPC doublets with strips in both projections for the low-p_T trigger, and one RPC triplet with strips in both projections for the high-p_T trigger.

From the processor logic point of view, a 2×2 CM low-p_T Pad and a 2×2 CM high-p_T Pad were simulated. The whole system was equipped with eight CM VME boards, four in the η projection and four in the ϕ projection, each housing a CM demonstrator ASIC, for a total of 192 electronics channels.

A second full-size trigger tower ($90 \times 270\text{cm}^2$), made of two low-p_T RPC doublets and of one high-p_T RPC doublet, with strips in both projections, was constructed and tested in the same beam line.

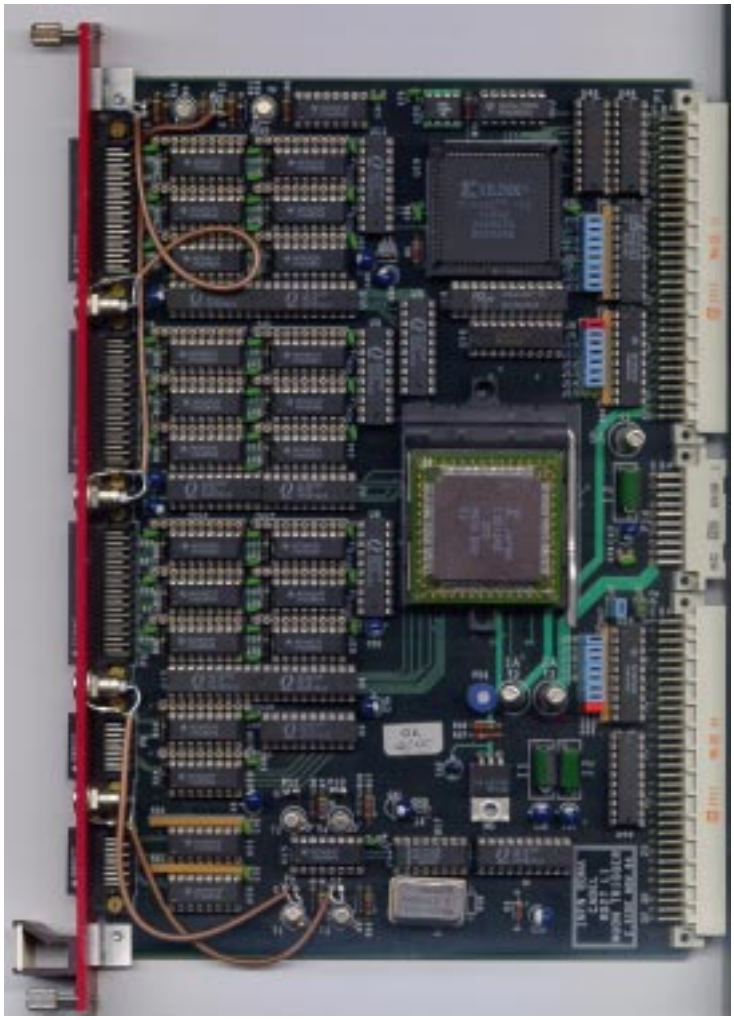

Figure 11-34 Coincidence-matrix board.

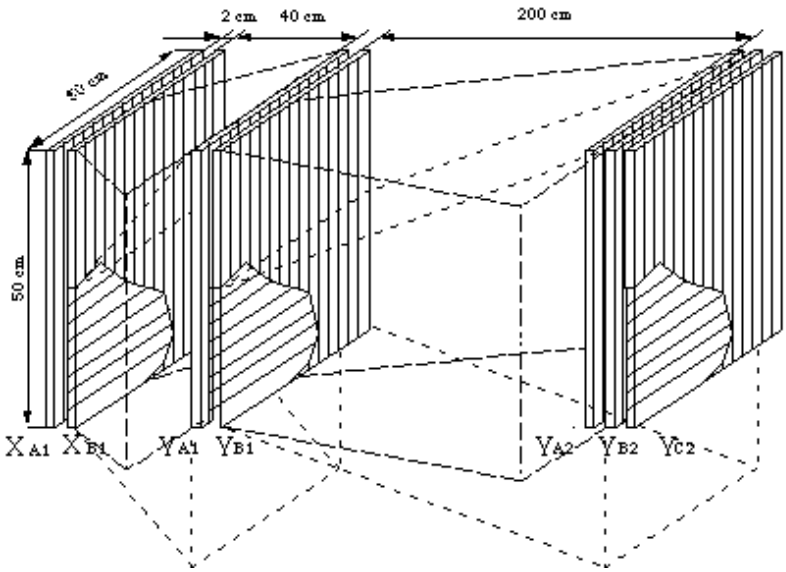

Figure 11-35 Reduced-size trigger tower.

Studies were performed for tracking, time resolution and efficiency. Data were taken with muons of 180 GeV, at 10, 50, 500 and 900 Hz/cm^2 beam fluxes. The LHC gamma background conditions were simulated through a 14 mCi ^{60}Co source, giving a 100 Hz/cm^2 background flux on the closest RPC [11-26], [11-27]. Results of the detector studies are documented in [11-8], Section 8.5.1. Concerning the trigger-processor studies, the results on tracking capability, trigger threshold behaviour and time resolution are in good agreement with the system design specifications. In particular, the excellent time performance of the system can be seen from Figure 11-36, where the processing time jitter of the level-1 trigger processor for low-p_T (dashed histogram) and high-p_T (full histogram) tracks is shown, for both X and Y coordinates. The average low-p_T processing time is subtracted so that the distribution is centred at t=0.

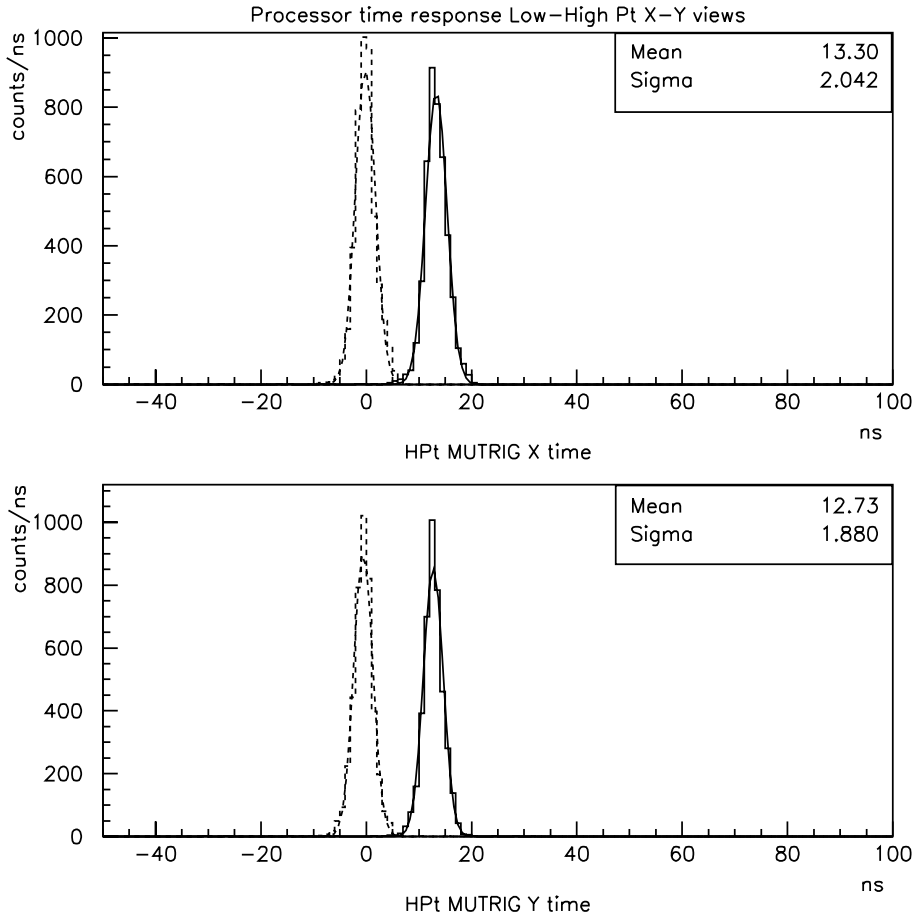

Figure 11-36 Processor time response for low- and high-p_T in both views.

11.4 Trigger system construction and assembly

The level-1 muon barrel trigger schedule has been worked out taking into account the necessity to follow the general schedule for construction, assembly, installation and integration of the ATLAS experiment. For each relevant component of the trigger system, a detailed schedule of the different phases and of the intermediate milestones was established on a quarterly basis (Figure 11-37). Following the schedule, the system should be ready to be pre-assembled on the chambers in the middle of 2002, allowing also for nine months of contingency.

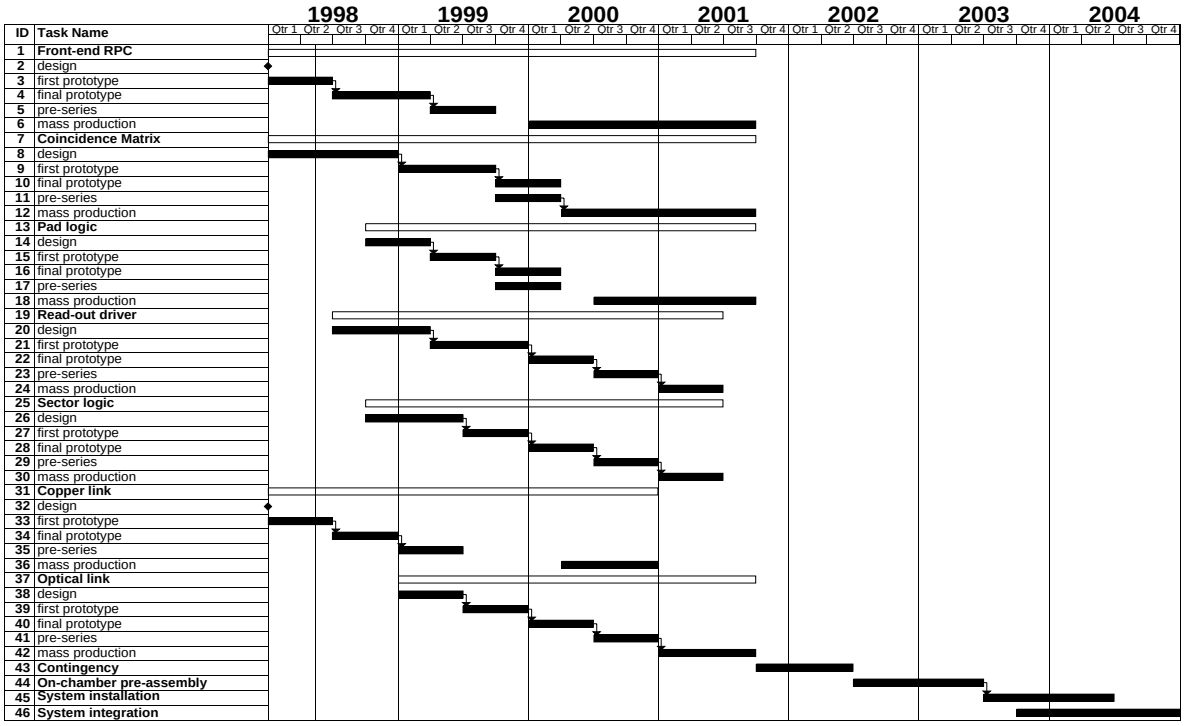

Figure 11-37 Level-1 muon barrel trigger schedule (The front-end electronics is part of the muon spectrometer.)

11.5 Quality assurance programme

The quality assurance programme is a relevant aspect in the implementation of our trigger system, since the system must work at least for 10 years in a very difficult environment, where the accessibility is very limited or in some cases even impossible. This means that a set of procedures and rules must be followed in the implementation of the trigger system to assure the required quality. The programme is summarized in Table 11-18.

As a first and most relevant aspect, it must be ensured that for the electronic system the requirements meet the physics goals. In this regard, we have produced a document, the Level-1 Muon Trigger User Requirements Document (URD), that is the basis for the design of the barrel trigger system.

Table 11-18 Quality Assurance programme summary

Requirements	URD document
Design	Preliminary Design Review followed by Interim Design Reviews if required
Development	Prototyping, iterate design, followed by Final Design Review
Production	Production Readiness Review (PRR)
Installation	Installation procedures and schedule set by ATLAS experiment
Quality and maintenance	Electronics Reliability Rules

The realization of the trigger system, that must be robust and adequately tested, should follow a set of rules (Table 11-18) that cover all aspects of the implementation chain.

Furthermore, we plan to use the following Electronics Reliability Rules:

- evaluation of allowable aggregate failure rate;
- evaluation of allowable replacement frequency for accessible components;
- suggested goal of <1% aggregate channel loss for a 10 year running cycle;
- in the design of ASICs, obtain from vendors data on defects / unit area for a given run process and use software-reliability tools to obtain the reliability of components;
- test all on-detector circuits to validate that they satisfy radiation-tolerance requirements;
- obtain for commercial components data from vendors and use Mean Time Before Failure software tools to evaluate the reliability of circuits;
- burn-in, at least for inaccessible components;
- ensure full availability of spare components and parts for a 10 year running cycle;
- define rules for access to fix problems and repair circuits in short- and long-term maintenance.

Before launching the construction of the major parts of the experiment, ATLAS has established to organize a Production Readiness Review (PRR). This review will cover design, integration, logistics, quality and safety issues, other than organizational matters. The items of the level-1 muon barrel trigger reviewed by a PRR and the corresponding dates at which the reviews will take place are shown in Table 11-19.

Table 11-19 Production Readiness Review schedule

Coincidence-matrix	April 2000
Pad Logic	July 2000
ROD and Sector Logic	February 2001
Optical link	January 2001

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