FINUDA

FRASCATI

ST03

8 channels common STop generator for the FINUDA experiment

USER'S MANUAL

The latest version of this manual is available on the web at:

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1. DESCRIPTION

1.1 FUNCTIONAL DESCRIPTION

The ST03 is a 1-unit wide VME 6U module performing discrimination, logic, gating and shaping functions on eight couples of inputs.
The functional diagram is shown in figure 1.
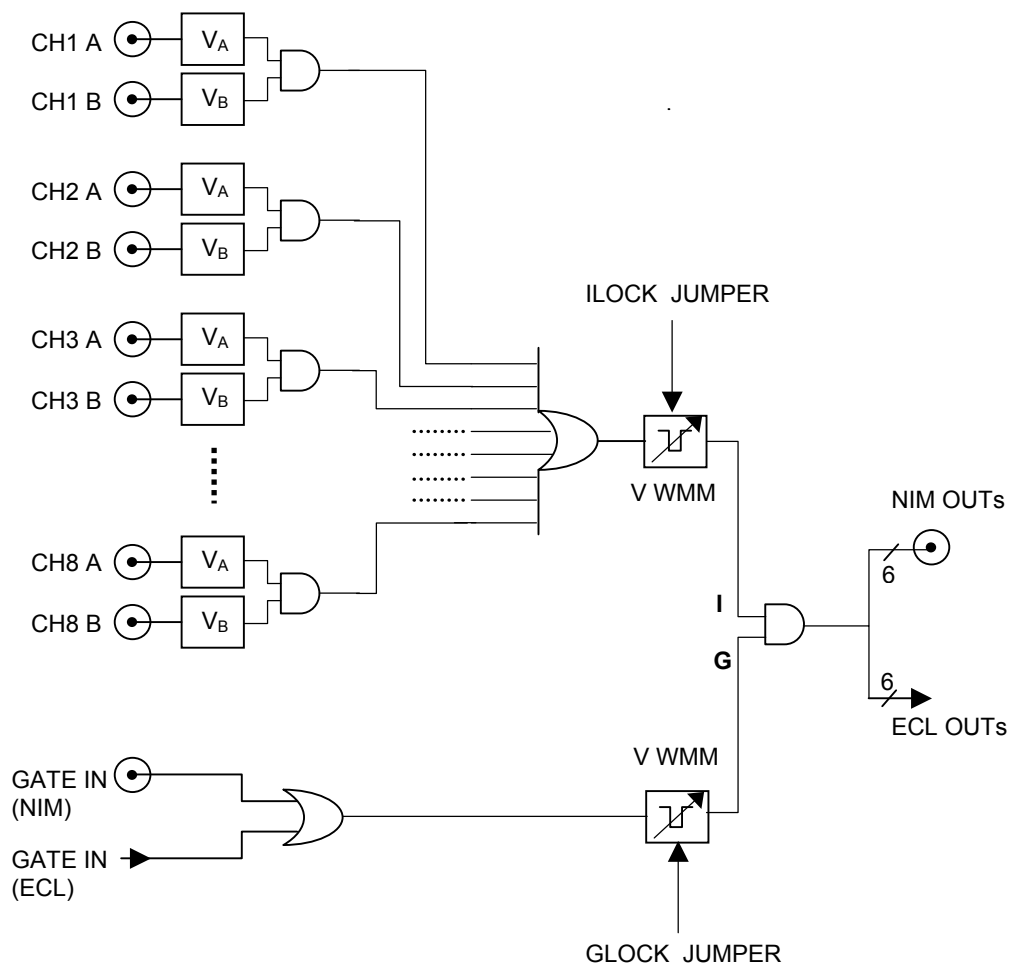

FIGURE 1

Each input channel is sent to a leading-edge discriminator. The thresholds V_A and V_B are common for two groups of eight channels (labelled A and B) and they are manually adjustable by means of two trimmers placed on board.

The OR of the AND of each couple of inputs is shaped into a fixed-width pulse by a Variable Width Monostable Multivibrator (VWMM). The pulse width can be adjusted in the range 5-64 ns using the OWIDTH trimmer placed on front panel.

The pulse can reach the outputs only if it is "in coincidence" with a "gate" signal. Two gate inputs (ECL and NIM) are provided on the front panel; the gate signal is shaped by a VWMM and transformed into fixed length pulse. The shaped gate width can be adjusted in the range 10-110 ns using the GWIDTH trimmer placed on front panel.

The shaped input and gate signal are sent to an AND gate performing the coincidence. Internal delays have been set in such way that if gate and input signal are simultaneously applied to ST03, the gate pulse reach the coincidence (AND) before the input pulse. This ensures that the output timing is only determined by the input signal leading edge. See chapters 2.5 and 3.6 for details.

The coincidence output is finally sent to a buffer circuitry providing 6 ECL outputs and 6 NIM outputs.

The purpose of ILOCK and GLOCK jumpers is described in chapter 3.3.

1.2 ST03 in the FINUDA experiment

Will be written in the next releases of this manual.

2. SPECIFICATIONS

2.1 PACKAGING

1-unit wide VME unit. Height: 6U.

2.2 EXTERNAL COMPONENTS

See Figure 2 for reference.

CONNECTORS

- Signal inputs
n. 8 double-LEMO connectors (CERN code: SCEM 09.46.11.186.0) for CH1A, CH1B inputs up to CH8A, CH8B. "A" inputs are on the left side of the front panel.
- Gate inputs
  - n. 1 single-LEMO NIM input
  - n.1 ECL input
- Outputs
  - n. 6 NIM outputs. Three double-LEMO connectors   (CERN code: SCEM   09.46.11.186.0) have been used. The outputs are independent from each other, hence no termination is needed for unused outputs.
  - n. 6 ECL outputs. Each output is separated from the other by two ground pins to allow the use of shielded twisted-pair cables and also direct measurements of output signals with a scope probe.

JUMPERS

Two jumpers labelled ILOCK and GLOCK are present on the front panel. See section 3.3 for operating details. Note that, in normal operating mode, both jumpers MUST BE shorted.

LEDs

- Power supply LEDs
Three LEDs light up when the required crate voltages are present. They are placed on the front panel bottom.
  - Green LED: -5 V
  - Red LED: -2 V
  - Yellow LED: +5 V

If one or two LEDs do not light up when the VME crate is ON, switch OFF the crate and remove ST03 from the bus. Check crate voltages and on-board fuses. See chapter 3.8 for details.

- Input LEDs
Each of the 16 inputs of ST03 has a LED indicating the presence of a valid input signal. An input signal is "valid" when exceeding the discriminator threshold. (V_A for CH1 A to CH8 A and V_B for CH1 B to CH8 B. See chapter 3.2 for threshold settings).
The LEDs light up for the whole duration of the input signal or they flash for 200ms if a very short input pulse is applied.
Input LEDs are yellow for "A" input and green for "B" inputs.
- Gate LED
A green LED flashes for 200ms whenever a gate pulse is applied to the gate inputs. It is steadily lit if GLOCK jumper is removed.
- Output LED
A yellow LED flashes for 200ms when a pulse is available at the outputs.

TRIMMERS

- OWIDTH
Output pulse width. Range: 5-64 ns
See section 3.5 for setting procedure.
- GWIDTH
Gate pulse width. Range: 10-110 ns
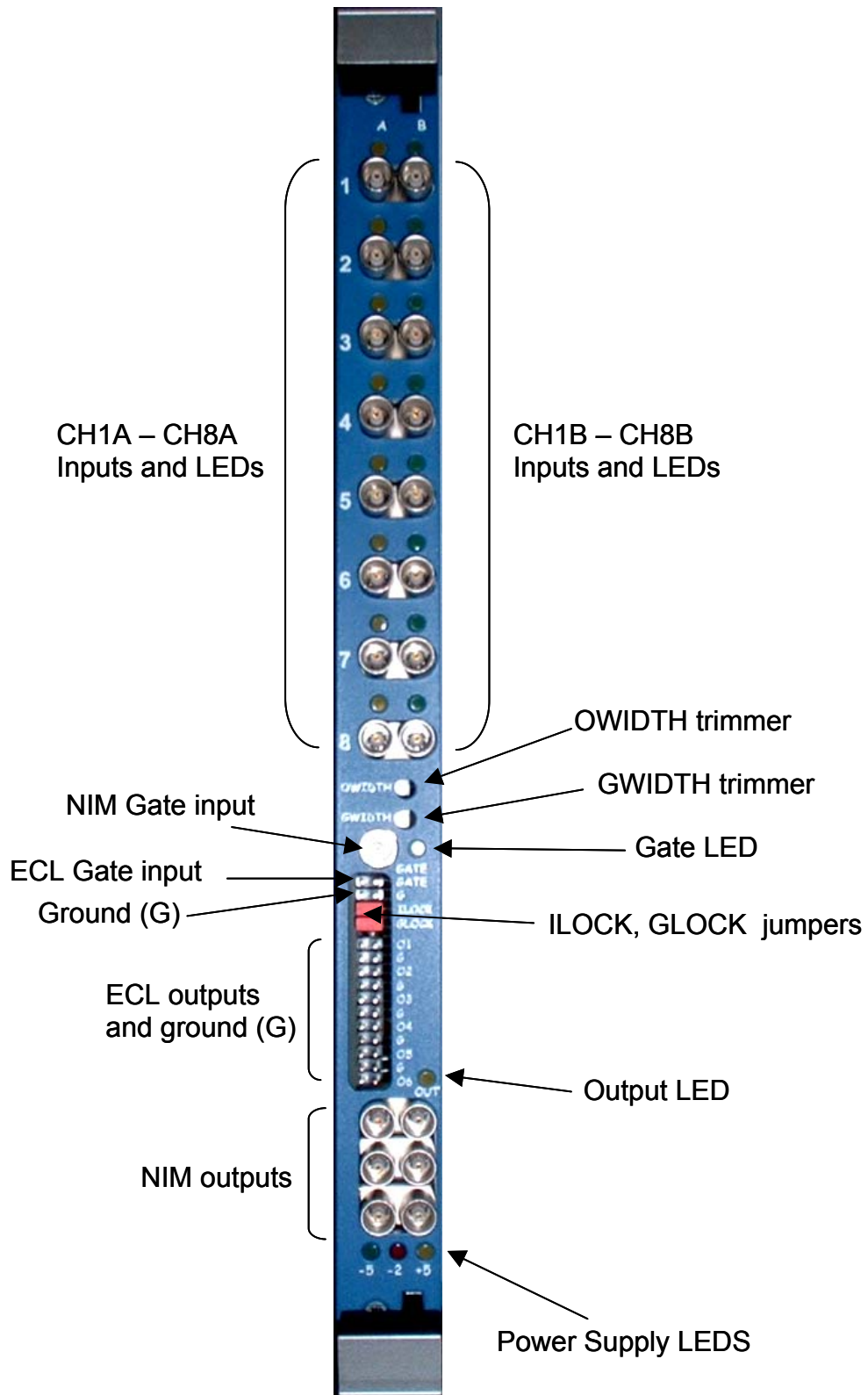See section 3.4 for setting procedure.

FIGURE 2 – ST03 Front Panel

2.3 INTERNAL COMPONENTS

TRIMMERS

The on-board trimmers R207, R208 allow fine regulation of threshold voltages V_A and V_B respectively. See section 3.2 for details.

FUSES

F1: T 2A

For boards with prototype area unmounted (S/N 001):

F2, F3: T 3A

For boards with prototype area mounted (S/N 002):

F2, F3: T 4A

2.4 INPUT SIGNALS CHARACTERISTICS

INPUT CHANNELS

Accept any input voltage in the range –2V to +3V.

(NOTE: the board S/N 001 accepts only from 0V to -2.5V). The voltage difference between input and threshold MUST NOT exceed 3.7V.

Minimum width: 5 ns.

GATE INPUTS

- n. 1 ECL input, 110Ω terminated, min. width 5 ns.
- n. 1 NIM input.

2.5 PROPAGATION DELAYS

The following values have been measured with 1 ns leading-edge input signals and thresholds set to –350mV. Note that <u>using input signals with slow leading edges may significantly increase the propagation delays.</u>   See section 3.6 for timing measurement details.

- Inputs to NIM outputs (Tio_N): .... 7.0 ns.
- Input to ECL outputs (Tio_E): .... 6.2 ns.
- NIM Gate to NIM outputs (Tgo_{NN}):.. 4.8 ns
- ECL Gate to NIM outputs (Tgo_{EN}): .... 5.3 ns
- ECL Gate to ECL outputs (Tgo_{EE}): .... 4.3 ns
- Gate lead at coincidence with NIM gate (Tig_N):....................... 2.2 ns
- Gate lead at coincidence with ECL gate (Tig_E):....................... 1.9 ns

The "Gate lead at coincidence" is the lead of the gate signal "G" respect to the input signal "I" at the coincidence input (see fig. 1 and chapter 3.6).

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2.6 POWER REQUIREMENTS

For boards with prototype area unmounted (S/N 001):

- +5.0 V   0.5 A
- -5.2 V   1.3 A
- -2.0 V   1.1 A

For boards with prototype area mounted (S/N 002):

- +5.0 V   0.6 A
- -5.2 V   TBD
- -2.0 V   TBD

3. HARDWARE DESCRIPTION

3.1 INTRODUCTION

ST03 has been designed with the main target of jitter minimisation. The goal has been achieved by means of the following design choices:

- *Fully differential design.*
- *Precise input comparators.*
- *Low-noise voltage references.*
- *ECLinPS logic with very fast rise/fall times ($\approx$ 200 ps).*
- *Adapted differential PCB tracks and proper layout*

3.2 THRESHOLDS SETTING

The threshold for channels "A", V_A, is set by potentiometer R207, placed near the VME connectors; the threshold for channels "B", V_B, is set by potentiometer R208.

To read thresholds, take a DVM with high input impedance   ($Z_{IN} \geq 1M\Omega$) and put the probes on the test-point pads labelled "GND" and "VREFA" (or "VREFB" for measuring V_B).

When working with NIM signals, a 350-400mV threshold is recommended.

The voltage references mounted on ST03 boards S/N 001 and 002 allow a thresholds setting in the range 0V to -2.5V.

In principle, mounting all components shown in the schematic (see sheet 10/15 - "Power and voltage references") and choosing LM4051-2.5 or ZRA250F01 for U44, U45, U46, U47 it is possible to set thresholds in the range –2.5V to +2.5V. In this case, it is also possible to discriminate TTL levels (the 47Ω input termination should be removed).

<u>Note that the voltage difference between input and threshold must not exceed 3.7V.</u>

3.3 ILOCK AND GLOCK JUMPERS

The main reason for these jumper is to allow measurements and calibration of ST03 with no need of putting the board on a VME extender to probe directly the board. Furthermore, they also allow you to use ST03 in a different way from that it has been designed for. For instance, removing GLOCK jumper, you can use ST03 as a simple signal shaper (pulse width adjustable with GWIDTH) with 6 ECL outs and 6 NIM outs.

In normal mode operations both jumpers should be closed.

The AND coincidence gate (see figure 1, pag. 4) has two inputs: "I", coming from input logic, and "G", carrying the gate signal.

When ILOCK jumper is removed, "I" is forced active regardless of input status. Hence, the shaped gate signal is directly sent to the outputs and can be viewed with a scope.

When GLOCK jumper is removed, "G" is forced active regardless of gate input status. Hence, the shaped signal produced by AND/OR input logic is directly sent to the outputs and can be viewed with a scope. In this state, the "GATE" led is lit.

3.4 GATE WIDTH MEASUREMENT AND SETTING

Remove the ILOCK jumper and connect a pulse generator to the gate input (NIM or ECL). Watch the output with a scope: what you see is exactly the shaped gate signal "G" (see figure 1 pag. 4) as it enters the coincidence AND gate. Set the width by GWIDTH trimmer on front panel. Put back the ILOCK jumper in its place.

Figure 3 shows a measurement done on ST03 S/N 001. Track 1 is the NIM gate input and track 2 is the shaped gate at the NIM output (ILOCK removed). Timing is shown on the right side of the figure.
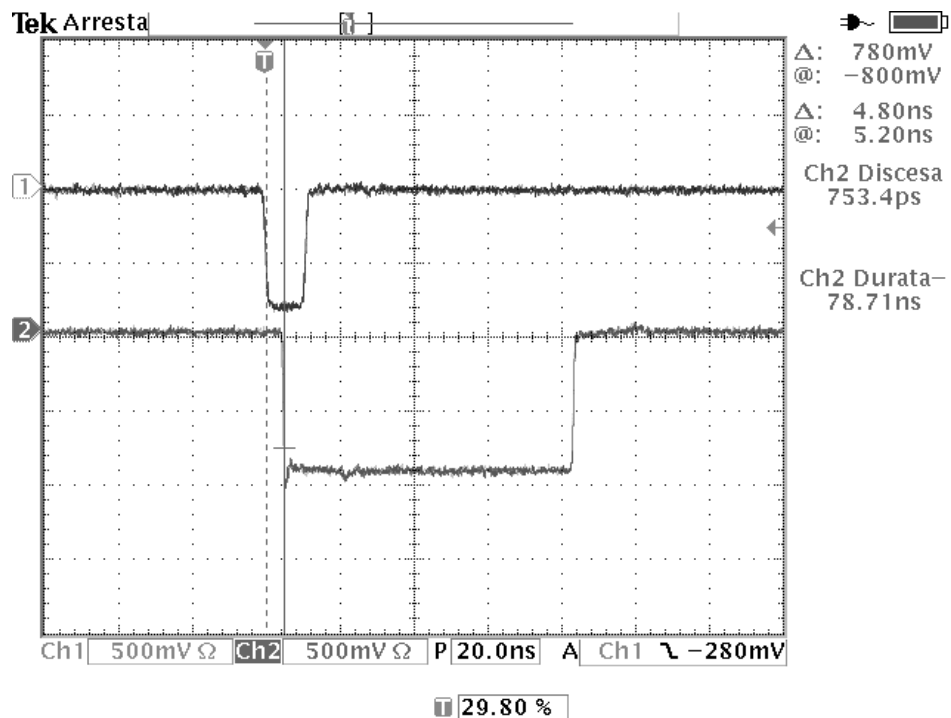

FIGURE 3 – Gate at the NIM input [1] and at the NIM output [2]

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3.5 OUTPUT WIDTH MEASUREMENT AND SETTING

Remove the GLOCK jumper. Remove any input signal. Connect a steady "high" NIM logic level on one input and a signal generator on the other input of the same channel (see chapter 3.7 to know how to generate a "high" NIM level). The input LEDs must light up. Watch the output with a scope: what you see is exactly the shaped signal "I" (see figure 1 pag. 4) as it enters the coincidence AND gate. It is also the signal that you get from the outputs in the normal operating mode. Set the width by OWIDTH trimmer on front panel. Put back the GLOCK jumper in its place.

Figure 4 shows a measurement done on ST03 S/N 001. Track 1 is the NIM input signal and track 2 is the shaped NIM output (GLOCK removed). Timing is shown on the right side of the figure.
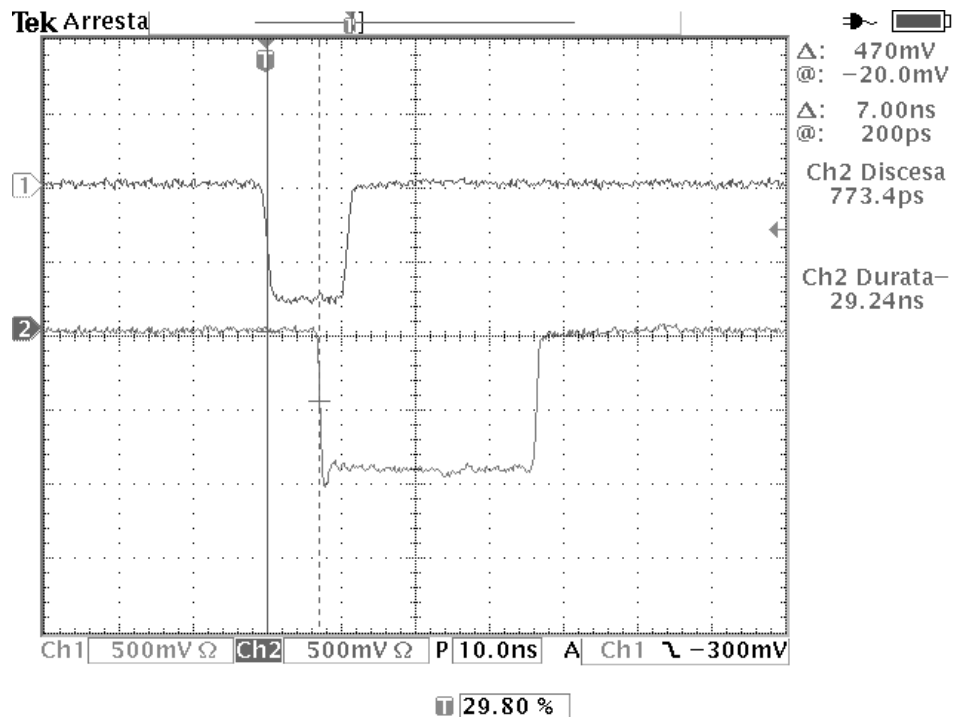

FIGURE 4 –NIM input [1] and NIM output [2]

3.6 DELAY MEASUREMENTS

The following procedure refers to NIM inputs and NIM gate. When dealing with other signal levels, remember the following:

- Set the proper threshold values if using analog input levels
- Take additional delays into account when using ECL/NIM converters to generate an ECL gate signal.

Furthermore, if you want to make precise timing measurement on ECL signals you should avoid the commonly used "ECL/NIM probe".

3.6.1 INPUT TO OUTPUT DELAY (Tio)

Connect a 50Ω splitter to the output of a signal generator. Set the output level to get NIM-compatible levels at the splitter outputs. Connect two 50Ω cables to the splitter outputs: one of length L and the other of length 2L. Connect the 2L-long cable to a channel of a scope.

Connect the L-long cable from the splitter to a ST03 input. Put a steady "high" NIM level to the other input of the same channel (see chapter 3.7 to know how to generate a "high" NIM level). Check that input LEDs are lit.

Remove the GLOCK jumper. Check that gate LED is lit.

Connect a NIM output to the other channel of the scope with a cable of length L.

The time delay between two traces is the input-to-output delay you want to measure.

Remember to put back the GLOCK jumper in its place when finished.

3.6.2 GATE TO OUTPUT DELAY (Tgo)

Connect a 50Ω splitter to the output of a signal generator. Set the output level to get NIM-compatible levels at the splitter outputs. Connect two 50Ω cables to the splitter outputs: one of length L and the other of length 2L. Connect the 2L-long cable to a channel of a scope.

Connect the L-long cable from the splitter to the NIM gate input. Remove the ILOCK jumper. Check that gate LED is lit (or flashing if generator frequency is low).

Connect a NIM output to the other channel of the scope with a cable of length L.

The time delay between two traces is the gate-to-output delay you want to measure.

Remember to put back the ILOCK jumper in its place when finished.

3.6.3 TIME ALIGNMENT OF COINCIDENCE INPUTS (Tig)

Internal delays have been set in such way that if gate and input signal <u>are simultaneously applied</u> to ST03, the gate pulse "G" reaches the coincidence before the input pulse "I". This time difference is called "gate lead at coincidence" or "alignment margin" Tig; it ensures that the output leading edge timing is only determined by the leading edge of the input signal.

- If you need to measure the time alignment between your gate and input signals, simply disconnect them from ST03 and measure their time shift Ts with a scope (Ts = T_{gate} - T_{input}). Then add Ts to the "gate lead at coincidence" Tig reported in chapter 2.5. That's all.

- You can also get a quick idea of your gate/input time alignment watching the output signal with a scope. If the output width is the same you set with the OWIDTH trimmer, you are sure that your input signal is completely inside the gate signal, i.e. it starts and ends while gate is active. This is the correct operating mode. Instead, if you see an output signal shorter than the value you set, it means that the input signal precedes the gate or that it ends out of the gate. In this case you need to apply proper delays to "move" the input pulse inside the gate window.

You don't need to measure the alignment margin Tig: it has been measured once and reported in chapter 2.5. However, if you want to repeat the measurements, read the following.

See figure 1. If Tg is the arrival time of the gate signal "G" at the coincidence and Ti is the arrival time of the input signal "I", the alignment margin Tig is Tig= Ti-Tg.

Both Ti and Tg are unknown but they are related to the input-to-output delay Tio and to the gate-to-input delay Tgo by the following relations:

$$Tio = Ti + T$$
$$Tgo = Tg + T$$

Where T is the time from coincidence to output. Hence, the alignment margin Tig is:

$$Tig = Tio-Tgo$$

Tio and Tgo measurement procedure is reported in 3.6.1 and 3.6.2; the values measured on ST03 S/N 001 are reported in chapter 2.5 (page 9) for most I/O combinations.

3.7 HOW TO GENERATE A STEADY "HIGH" NIM LEVEL

Take an ECL-NIM converter and connect ch. X ECL input to ch. Y ECL output but with <u>opposite polarity.</u> In this way the LOW level present at the output will be read as HIGH by the ECL input. Therefore, a steady HIGH NIM level will be present at the ch. X NIM output.

3.8 TROUBLESHOOTING

ONE ORE MORE POWER LEDs DO NOT LIGHT UP
- Remove ST03 from crate and check crate voltages.
- Check the on-board fuses F1, F2, F3, placed near the JAUX connector.

THE OUTPUT SIGNAL IS NOT PRESENT
- Check that both input LEDs of at least one channel are lit. If not, check input signals and threshold values.
- Check that gate LED is lit. If not, check the gate input.
- Check that output LED is lit. If both input LEDs and gate led are lit, it may mean that gate and signal are not in coincidence. Check input and gate with a scope.

THE GATE LED IS ALWAYS LIT
- Check that GLOCK jumper is well-inserted in its place

THE OUTPUT LED DOES NOT LIGHT UP BUT THE OUTPUT SIGNAL IS PRESENT
- Measure the output width. If it is of the order of a few nanoseconds, it means that you have a very critical gate/input timing. If the gate/input superposition time is less than 6 ns, it can be large enough to generate a short output pulse but not enough to light up the output led. Check timing and put proper delays to recover the problem.

4. SCHEMATIC DIAGRAMS