Automated sixteen channels wire tension measurement system

A. Balla, P. Ciambrone, G. Corradi, G. Felici, G. Paoluzzi, B. Ponzio, V. Russo, M. Santoni, M.C. Spitalieri

Laboratori Nazionali di Frascati dell'INFN, Frascati, Italy

A. Nedosekin, V. Kulikov

Institute of Theoretical and Experimental Physics, Moscow, Russia

Abstract

A system to measure the wire tension of MDT tubes is presented. The system can measure up to sixteen tubes at the same time. It includes HV power supplies and modulators to excite mechanical oscillations around the wire fundamental harmonic resonance as well as an RS 232 interface for computer communications. The system is fully operated by a PC LabVIEW program.

1 Introduction

The electrostatic method for wire tension measurement was proposed by V. Kulikov [1]. The first system making use the method was designed at ITEP (Moscow) for the KLOE collaboration and was successfully used during KLOE Drift Chamber construction (more than 50,000 wires were checked at stringing time and at the end of construction) [2]. The system is also used for long-term monitoring of the KLOE Chamber deformation and wire tension stability.

The measurement method, as described in a previous ATLAS internal note [3], uses electrostatic force between wire and tube to excite mechanical oscillation around the wire fundamental harmonic resonance. The amplitude of the oscillation is sensed by measuring the capacitance variation in the wire-tube system using an LC oscillator (the sensor) coupled to the wire via a high voltage capacitor.

By measuring the sensor oscillation frequency when the high voltage is ON and OFF it is possible to determine the oscillation amplitude. Changing the high voltage modulating frequency an excitation curve of mechanical resonance is produced. The resonance frequency is obtained by fitting the resonance curve.

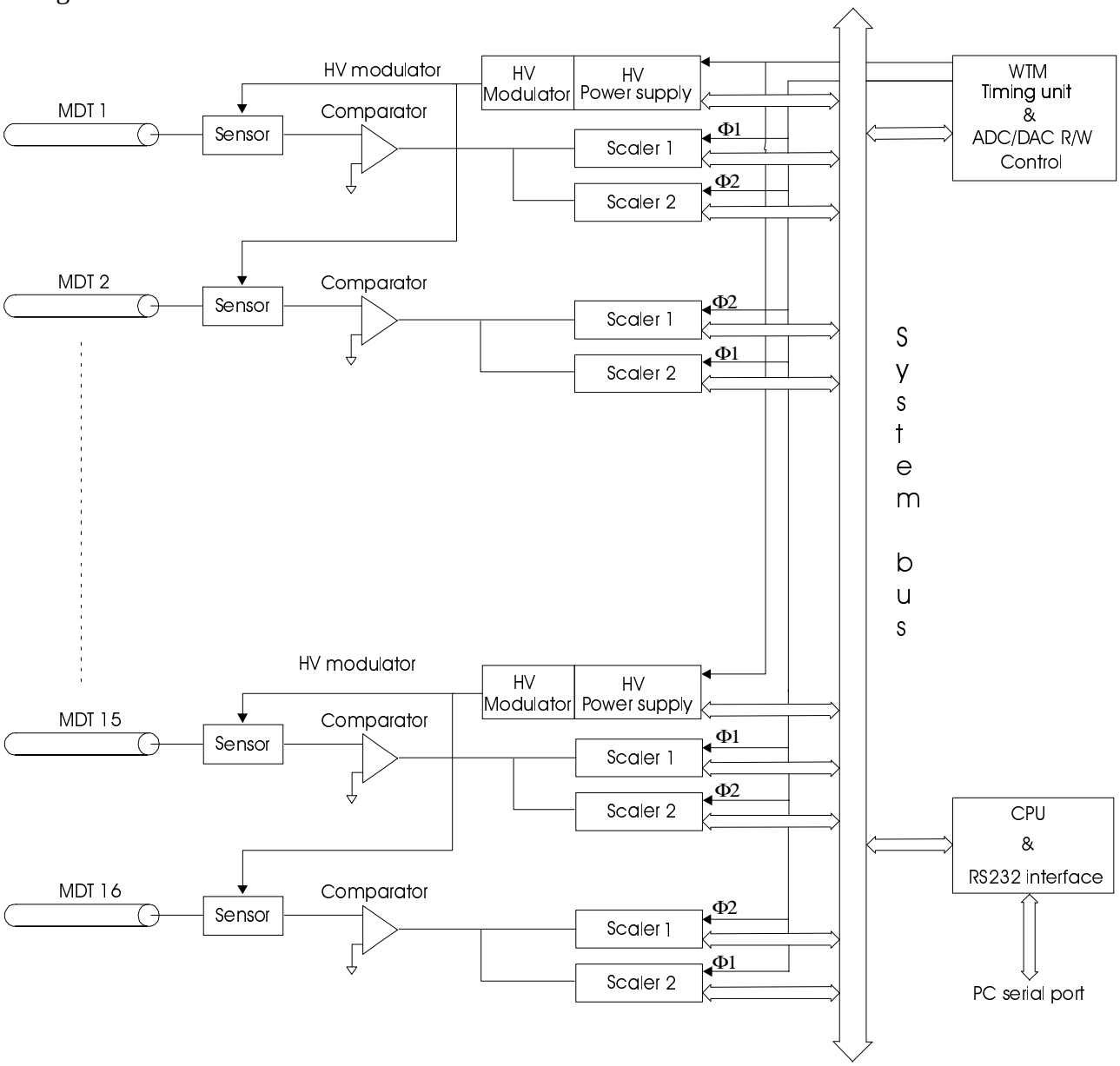

Figure 1 : WTM system block diagram

2 Wire Tension Meter (WTM) block diagram

The main system components are shown in fig. 1. Each sensor is connected to the measuring system through two cables. The first one (RG59) brings the HV modulated signal to excite wire mechanical oscillation, while the second one (RG174) is used both to supply the power to the sensor and to bring back to the measuring system the sensor output. The sensor output (a sinusoidal waveform) is discriminated (using zero crossing discriminators) and sent to the scalers. A dedicated circuit generates all the timing signals for the measurements as well as the control signals for HV generators setting/sensing. The system is managed by a computer running a LabVIEW[1] program through a serial RS 232 interface. A local processor supervises both communications and system measurement parameters setting.

3 WTM circuit description

The system main components are :

- The sensor circuit.
- The discriminator circuit.
- The scaler circuit.
- The timing unit.
- The local processor and RS232 interface.
- The low voltage power supply.
- The high voltage power supply.

In the following a short description of these components is given.

4 WTM sensor

As already said before, to check the mechanical wire tension we measure the resonant frequency of the wire by sensing the capacitance value of the wire-tube system. This is done using the LC oscillator circuit shown in fig. 2.

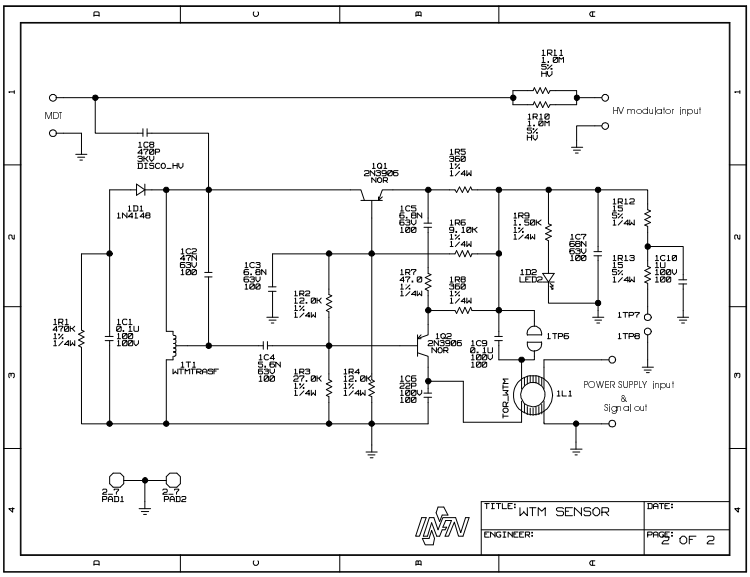

Figure 2 : WTM sensor circuit

[1] LabVIEW (trade mark of National Instruments)

Without the tube stray capacitance (about 28 pF) the circuit oscillates at a frequency of about 20 MHz (as we will see in the next sections, we do not need the sixteen sensors oscillate at the same frequency). When we connect the tube under test to the sensor and turn on the HV modulator, the sensor output frequency will change as a function of the wire distance from the tube wall. A transformer in the output section allows us to bring both signal and power by means the same (RG174) cable.

5 Discrimination and sensor power supply circuit

In this stage the sinusoidal sensor outputs are converted in digital square waves before sending them to the scaler circuit. In addition the same line which bring the signal is used to power the sensor. The circuit diagram for eight channels is shown in fig. 3.

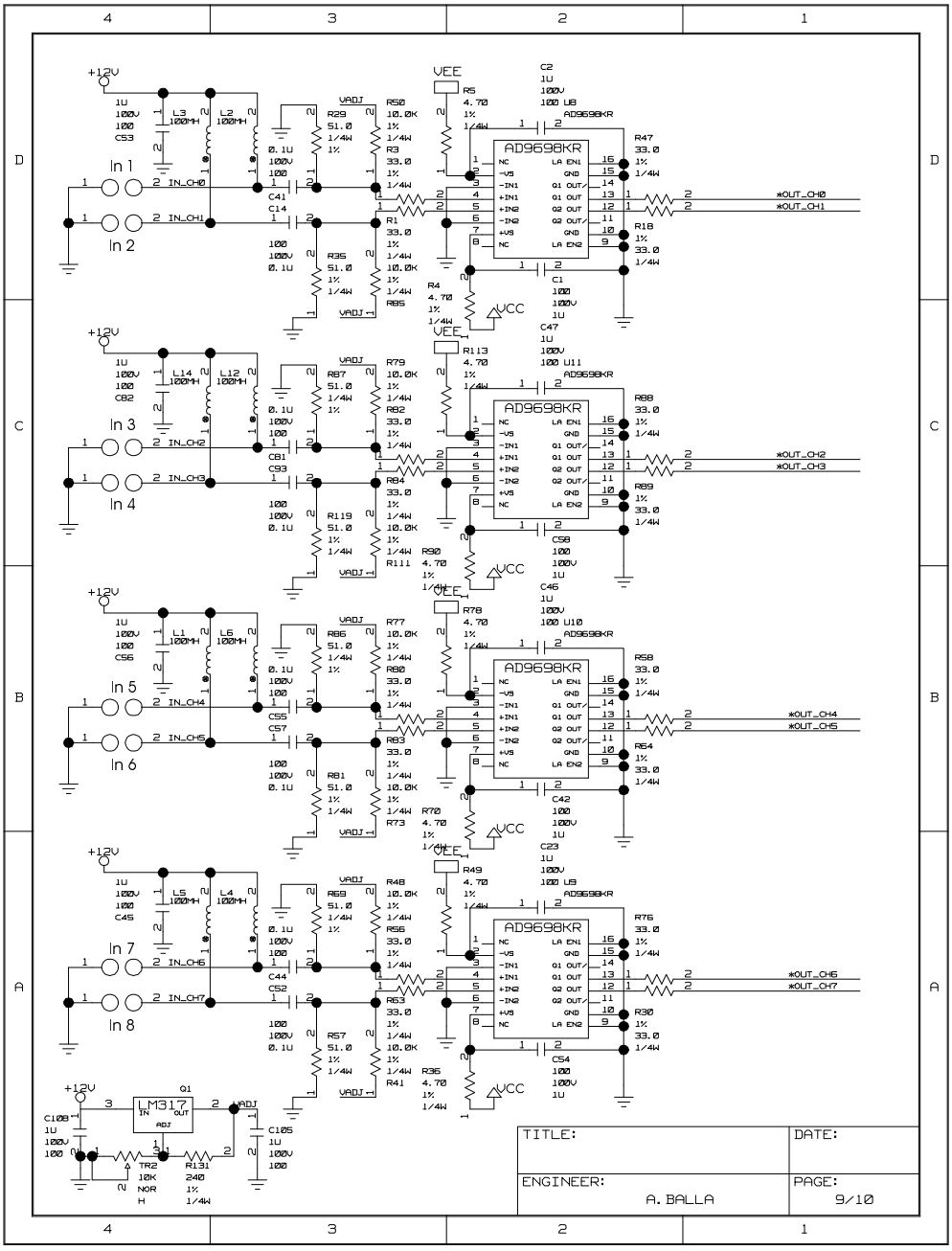

Figure 3 : Eight channels comparator circuit

Zero crossing comparators discriminate the AC coupled sensor signals, while a suitable value of inductance for each input allows to power the sensors without affecting the input signal amplitude.

6 Scaler circuit

As explained before, the sensor change his output frequency according to the HV modulation phase. As soon as the modulation frequency comes closer to the wire-tube system resonant frequency (about 37 Hz for 3.8 m MTDs) the capacitance value difference corresponding to the two HV phases (ON or OFF) increase. As a consequence also the sensor output frequency difference is increased.

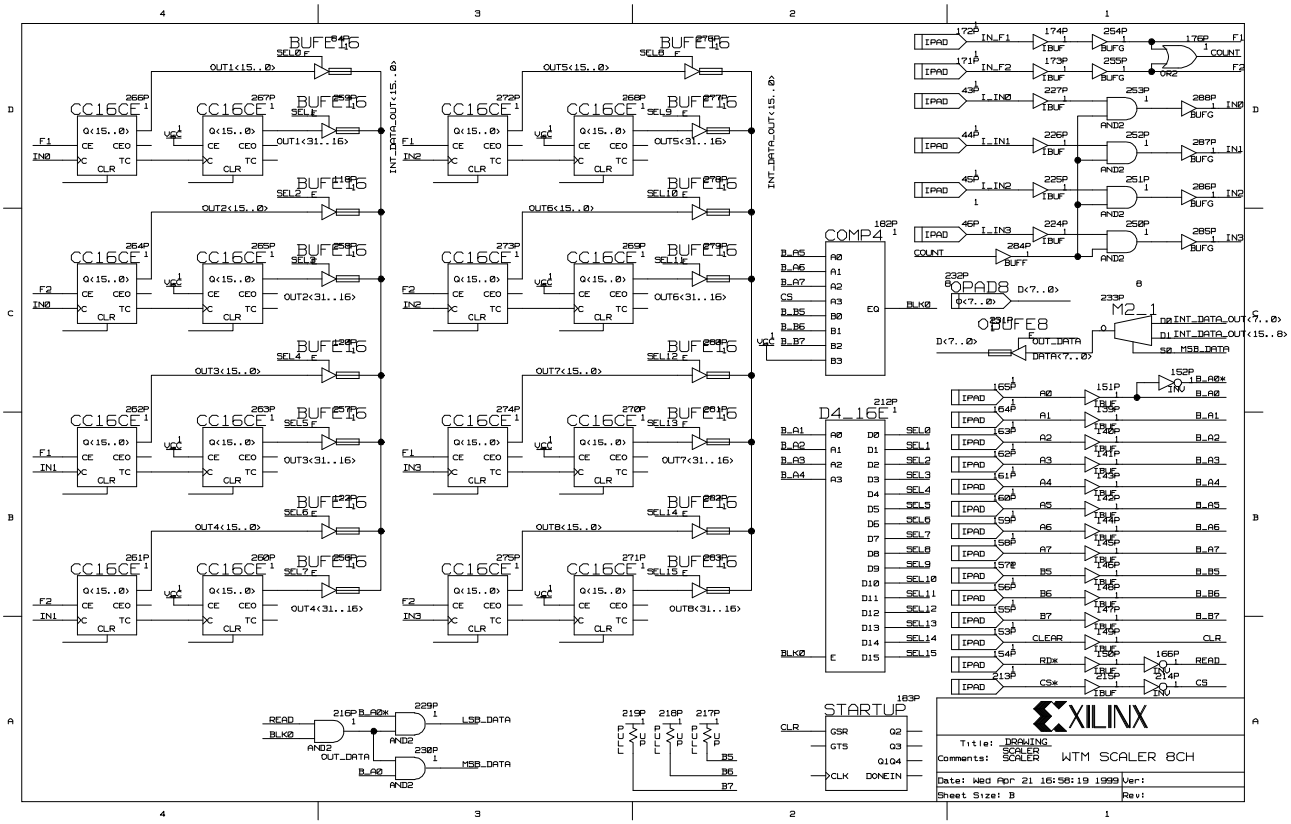

Figure 4 : Four channels scaler circuit

The circuit of fig. 5 measures this difference by counting the periods of sensor frequency outputs for both phases of the modulation frequency (F1 and F2); then, as already said before, slight differences in the sensors output frequency do not have an influence on the measurement.

Up to eight thirty-two bits counters have been packaged in a 4010 Xilinx FPGA together with the logic for device addressing and counters readout; then four FPGA have been used to implement the sixteen WTM scalers.

7 WTM timing unit

The WTM timing unit FPGA generates all the timing signals for the ADC/DAC read/write operations and for the wire mechanical tension measure. The block diagram of the section which manages the wire tension measurement is shown in fig 5. A 16.8 MHz quartz clocks a settable frequency divider to generate the HV modulation frequency. The output signal drives the block

where signals for scalers control are generated and delayed (these signals must be shifted by 90 degrees out of phase of HV modulation frequency). A further block allows the fine delay setting for both phases of modulation frequency (F1 and F2) to allow compensation for HV cable length. Lastly, a circuit has been foreseen to set the number of measurements for each HV modulation frequency; this option allows to speed the measurement avoiding frequent access from PC LabVIEW control program.

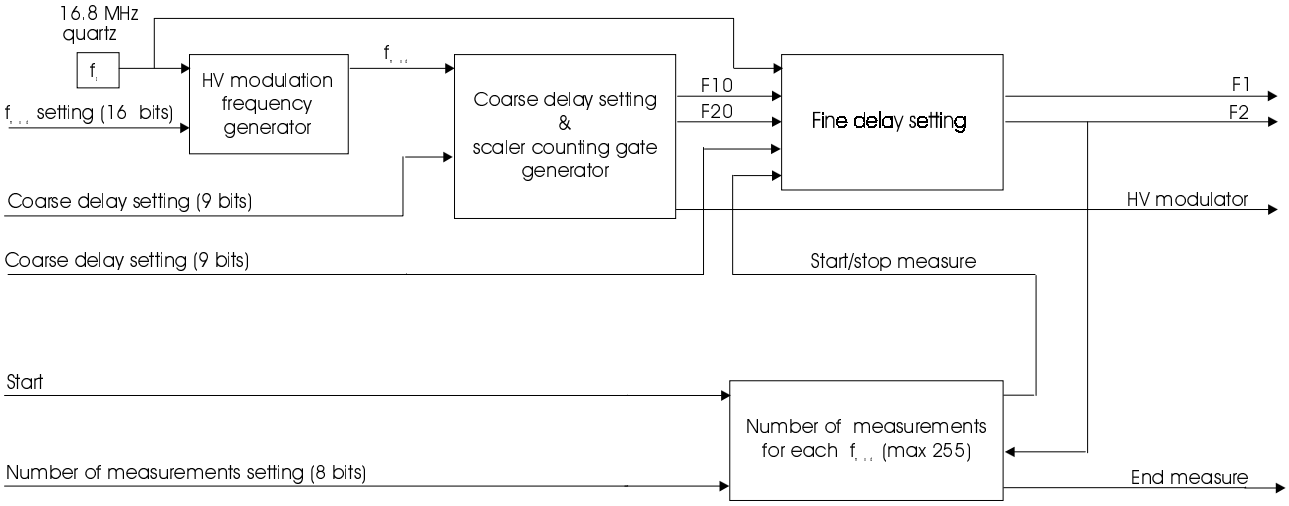

Figure 5 : WTM timing generator block diagram

8 WTM FPGA timing generator circuit diagram

Fig. 6, 7, and 8 show the diagram of the WTM timing circuit. Starting from fig. 6, the 16.8 MHz input clock (CLKI) is divided through the free running counter CC16CLE by the D<15..0>

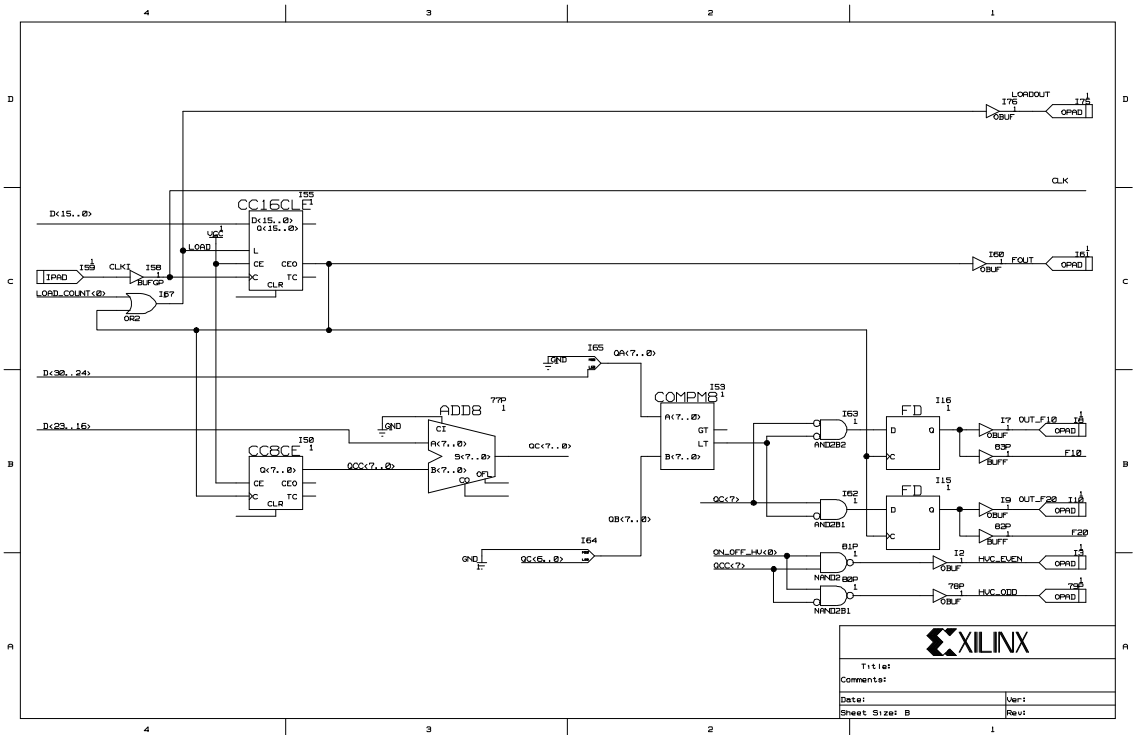

Figure 6 : HV modulation frequency and scalers enable signals generator

binary value factor, the minimum output frequency being (about) 256 Hz A lower frequency, together with a coarse delay for the output signals (OUT_F10 and OUT_F20) is obtained through the combination of the CC8CE counter, the ADD8 adder and the COMP8 comparator.

Assuming D<23..16> equal to zero, when QCC<6..0> is equal or bigger the D<30..24> value one of the two AND2B1 or AND2B2 outputs go HIGH (depending on the QC<7> status). Because the OUT_F10 or OUT_F20 signals end when QC<7> change its status, the value of D<30..24> sets both the width and the delay to the output drive counting gates with respect to QC<7> timing. The setting resolution is ≈ 4 ms and the maximum delay is ≈ 246 ms (4 ms • 63).

According with the status of HV ON/OFF bit, HVC follows QCC<7> status; so if D<23..16> is different from zero (but less than D<30..24>) both OUT_F10 and OUT_F20 pulses are moved inside QCC<7> width.

To sum up, if the value of D<23..16> is different from zero, but less than D<30..24>, D<30..24> bits set the pulse width, while D<23..16> bits set the pulse position with respect to QCC<7> waveform. Both OUT_F10 and OUT_F20 pulses are synchronised to the CC16CLE CEO output rise time by means the two FD.

The measure is started by the START signal (fig. 7); it loads the CC8CLED counter with the number of measurements for the selected excitation frequency (max 255) and enable the two AND2 gates. At the end of the counting the CEO output of CC8CLED goes HIGH finishing the measure.

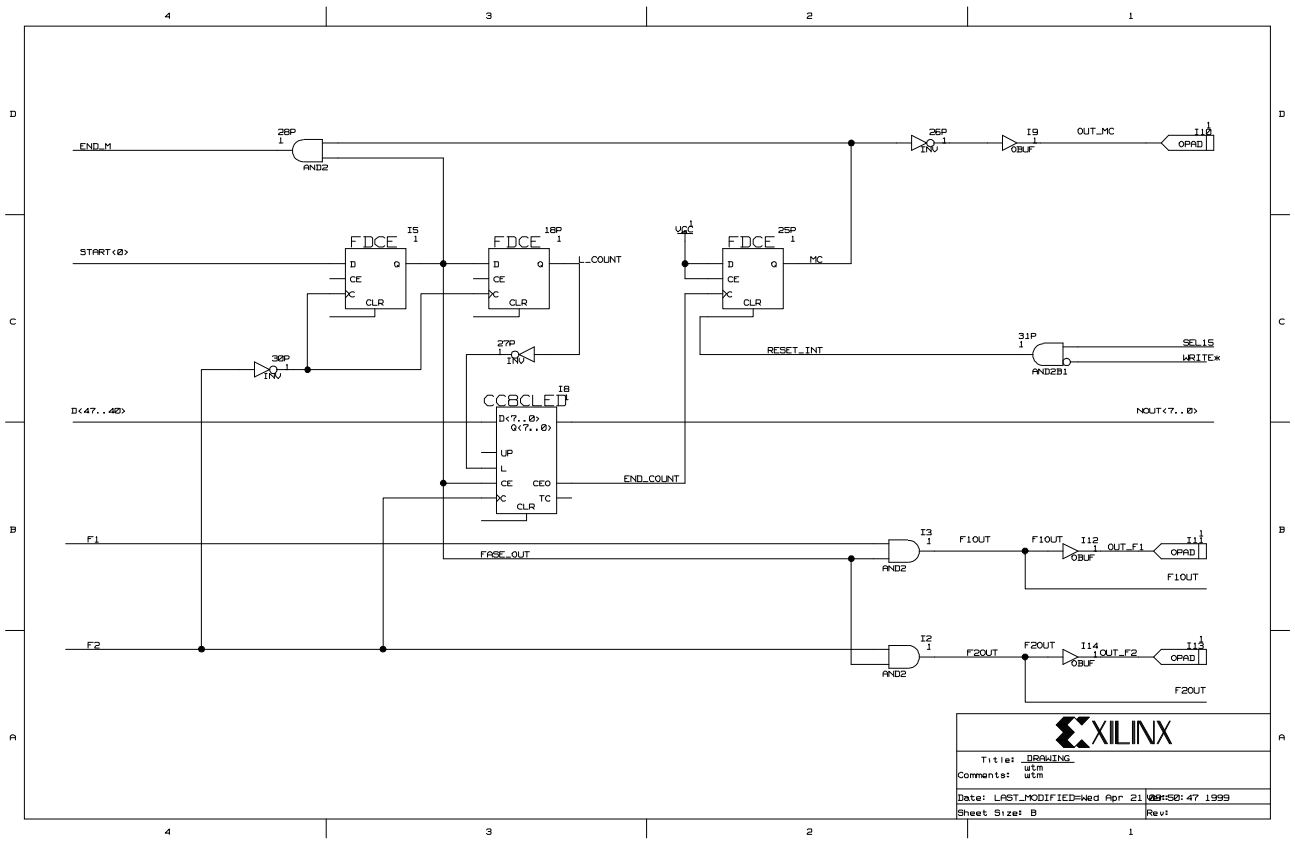

Figure 7 : measure control circuit

A fine adjustment of the F1 and F2 delay is carried out with the circuit of fig. 8. The CLK signal is used to clock the CC8CE counter; a multiplexer (M8_1E) allows to select one of the CC8CE outputs according to the status of the D<32..34> bits. Three shift registers (two SR16CE and one M2_1E) are used to obtain 32 different delay of the scaler F10/F20 enable signals trough the D<35..39> selection bits.

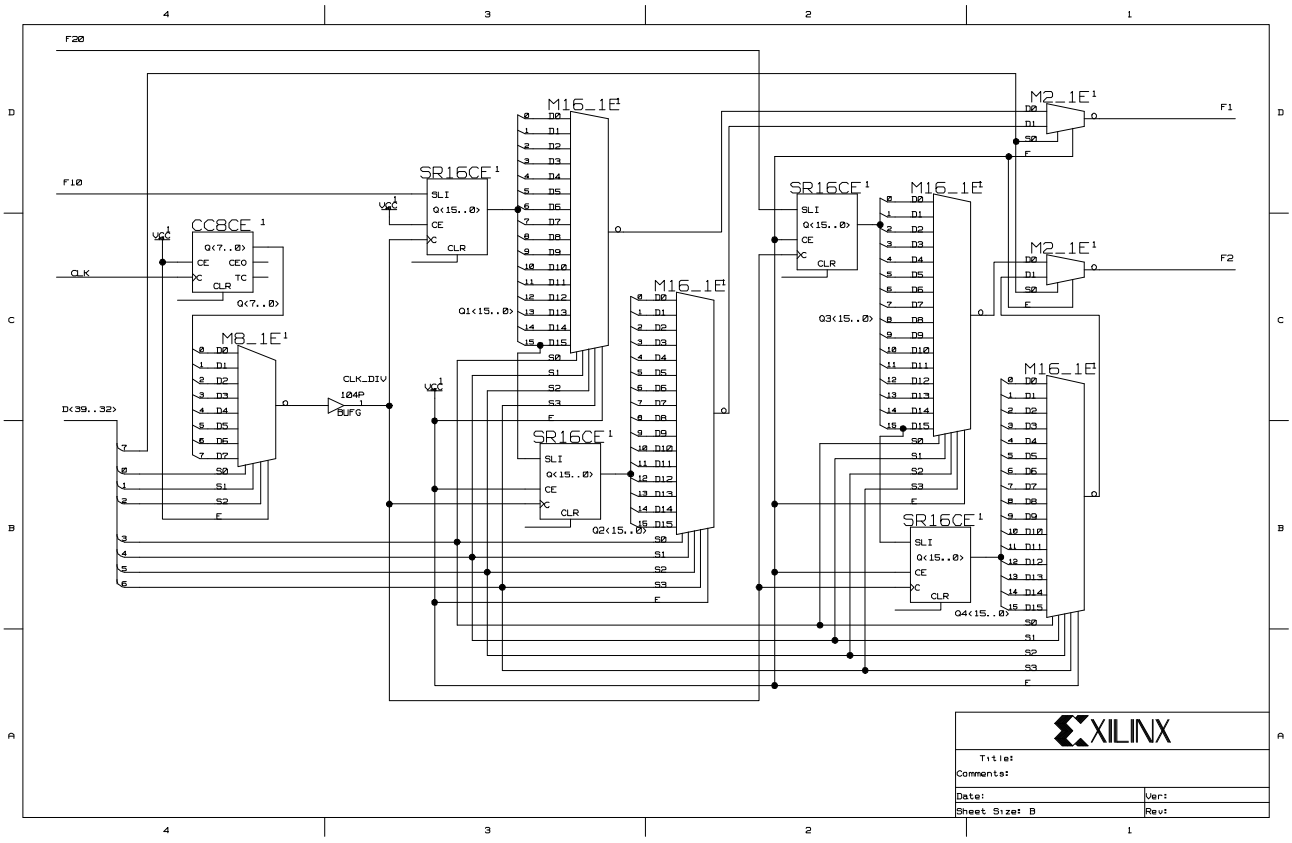

Figure 8 : fine delay setting circuit

Fig. 9 shows the simulated WTM timing circuit output waveforms. The START signal begins the measure starting the HV signal modulator and the two scalers enabling signals OUT_F10 and OUT_F20 with the selected coarse delay. The effect of circuit of fig. 8 (fine delay setting) are shown in the OUT_F1 and OUT_F2 waveform; after the last measure (the sixth in our case) an END_M signal is generated to begin data readout.

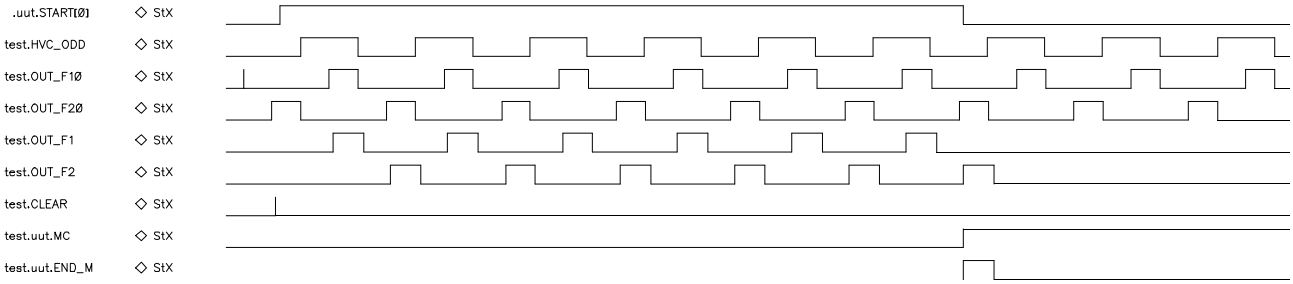

Figure 9 : WTM timing circuit output waveform

9 Local processor and serial RS232 interface

An internal 87C520 processor (fig. 10) manages the system operations and the RS232 PC interface. The use of a processor (we have used a 8051 core version of the Intel family processors) adds large flexibility both to the system control logic and to the external interface.

The serial interface works at a baud-rate of 57600 and has been designed in such a way that up to 100 different system (using the same interface) can be connected to the same serial line minimising external connections. Table 1 shows the serial protocol used to receive and transmit data from/to the system.

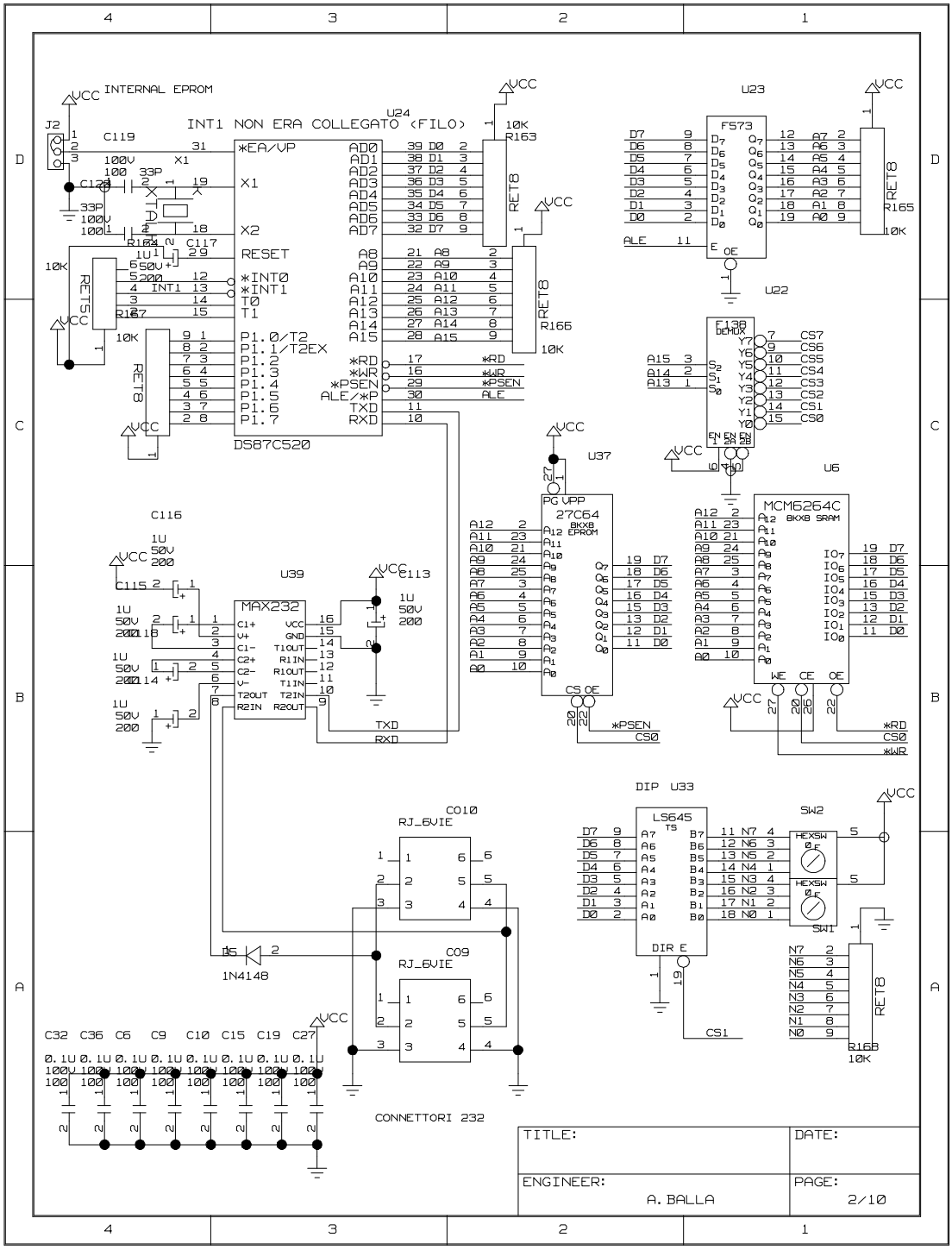

Figure 10 : Local processor and serial RS232 interface

Transmission Protocol (master to slave)	
<XX>	CPU slave number (from <01> to <FF>)
<XX>	Command <FF> (write) <00> (read)
<XX>	Address (<00> to <FF>)
<XX>	Data (<00> to <FF>)
(plus Carriage Return and line feed)	
Reception Protocol (slave to master)	
<XX>	CPU master number (<00>)
<XX>	Echo command (<FF> (write) <00> (read))
<XX>	Echo Address (<00> to <FF>)
<XX>	Echo data (write operation <00> to <FF>) data (read operation from <00> to <FF>)
(plus Carriage Return and line feed)	

Table 1: WTM RS232 serial interface protocol

10 Low voltage power supply

The voltage-current requirements for the circuit are summarized in table 2. Because of the small current required from +/- 5 V and –12 V, TO220 regulators are suitable to supply these lines.

The +12V power supply (fig. 11) uses a TIP127 transistor to increase the output current of the LM7812 voltage regulator (the transistor start to turn-on when the regulator output current exceed 200 mA), while step-down switching regulators are used to supply the HV switching power supply. This choice allows to reduce the power dissipation due to the HV generator supply current (about 8 A).

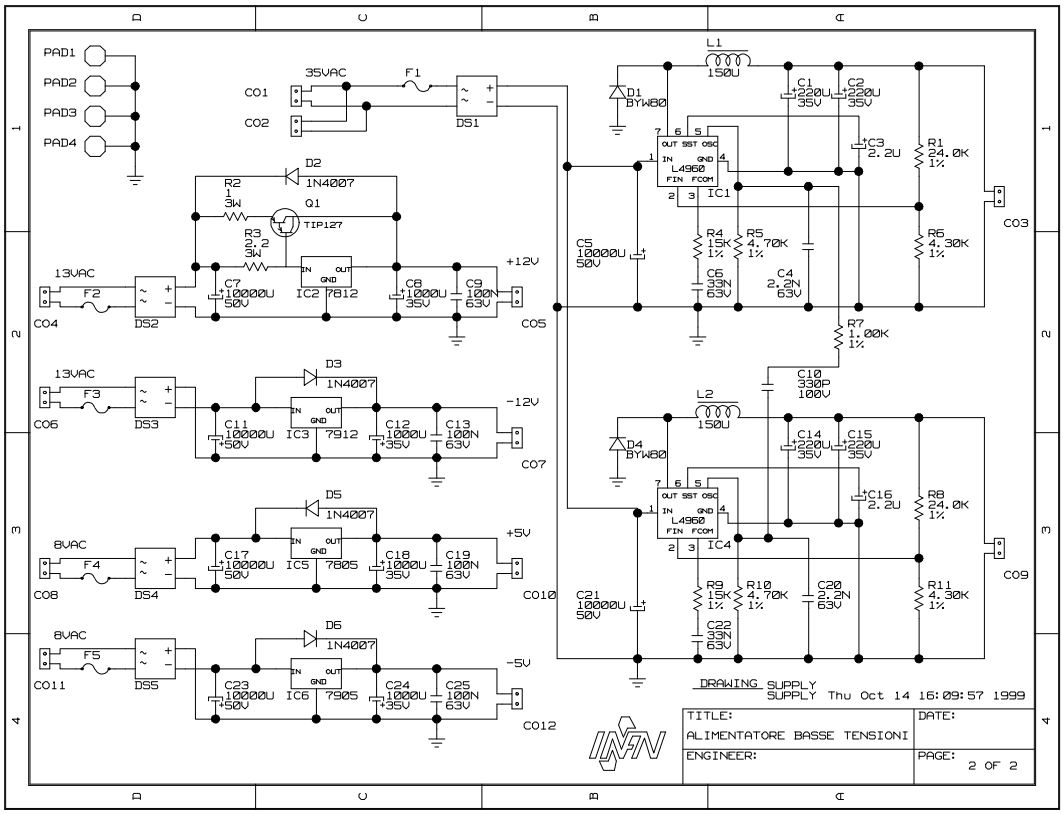

Figure 11 : Low voltage power supply

+5 V	1.2 A
-5 V	1.2 A
+12 V	3.5 A
-12 V	1 A
+36 V	4+4 A

Table 2: WTM system voltage/current requirement

11 HV power supply

Eight 7 mA 2 kV power supplies have been used to drive the sixteen HV modulator. The diagram of the HV power supply is shown in fig. 12. The HV power supply design has been optimised to get :

- low output noise;
- small dimension;
- high modularity.

Since the requirement on the output noise was the most critical, a sinusoidal 33 kHz waveform has been used to drive the transformer. This choice, together with an accurate design of final rectifier/multiplier stage allowed to reach a very low ripple.

The HV power supply main component is a Royer class converter (T1, Q4 and Q5) oscillating at a frequency resulting from T1 and C5 values (about 33 kHz). The transformer primary is composed by a 24+24 turns winding plus a 4 turns transistor bases control winding, while the secondary winding has 560 turns.

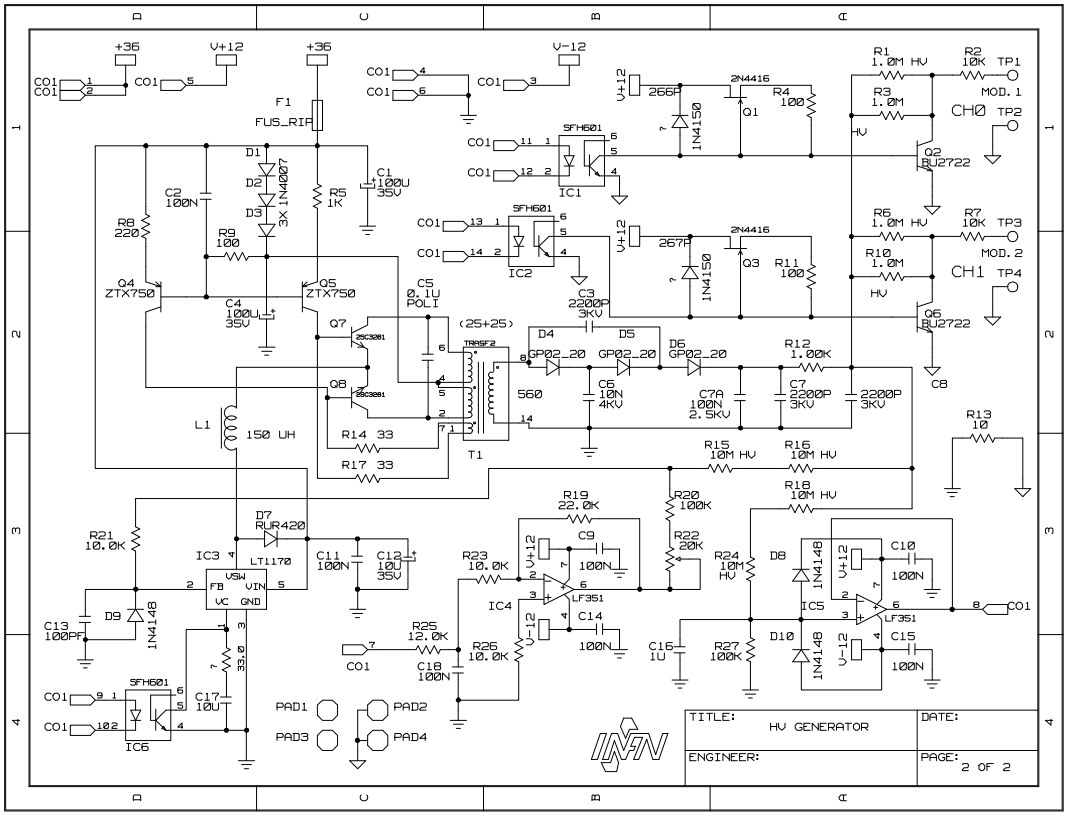

Figure 12 : High voltage power supply

A voltage tripler is used to rectify the sinusoidal output waveform; this trick allows to avoid insulating problems between primary/secondary windings and to reduce the primary/secondary stray capacitance improving the power supply noise characteristics.

Output voltage is stabilized closing the feedback loop on the FB LT1170 pin through the two 10 MΩ R15 and R16 resistors; this network is also used to set the output voltage in the 200 – 2 kV range (the limit on the minimum value of the output voltage comes from the necessity of minimizing the energy on primary winding to keep the same efficiency in the full output voltage range) through the IC4 operational amplifier (the circuit works as an active partition on the feedback voltage). A fraction of the filtered output is also available for the output voltage monitoring purpose through the IC5 operational amplifier.

Three optocouplers have been used in the circuit to isolate control logic; two of them (IC1 and IC2) are used to drive modulator, while the last (IC5) is used to turn on/off the switching regulator. Digital and HV ground are coupled through a 10 Ω resistor to minimize interference between digital and analog section.

12 The LabVIEW program

The WTM system is completely managed by a computer through a serial RS232 interface. The acquisition program has been carried out in the LabVIEW environment; fig. 13 shows the program control panel.

The measure is performed in parallel on 16 MDTs. Input parameters such as wire length, wire density, expected wire resonance frequency and frequency range are common for all tubes, while HV voltage values can be set independently for each couple of MDTs.

The measurement is performed by scanning the frequency range around the resonance with a step (in frequency) depending on the number of set-up points (step=frequency range / n-points). Last, the plot of the resonance curve and the relative fit for each single tube is made.

The results of the measurements (resonance curve amplitude, resonance frequency, and standard deviation) are shown (for each tube) in the LabVIEW control panel and stored in a temporary file where they can be readout from the database used to store all the chambers construction informations.

13 Acknowledgements

We would like to thanks Federico Bertino and Domenico Riondino for their help in the system printed circuits carrying out.

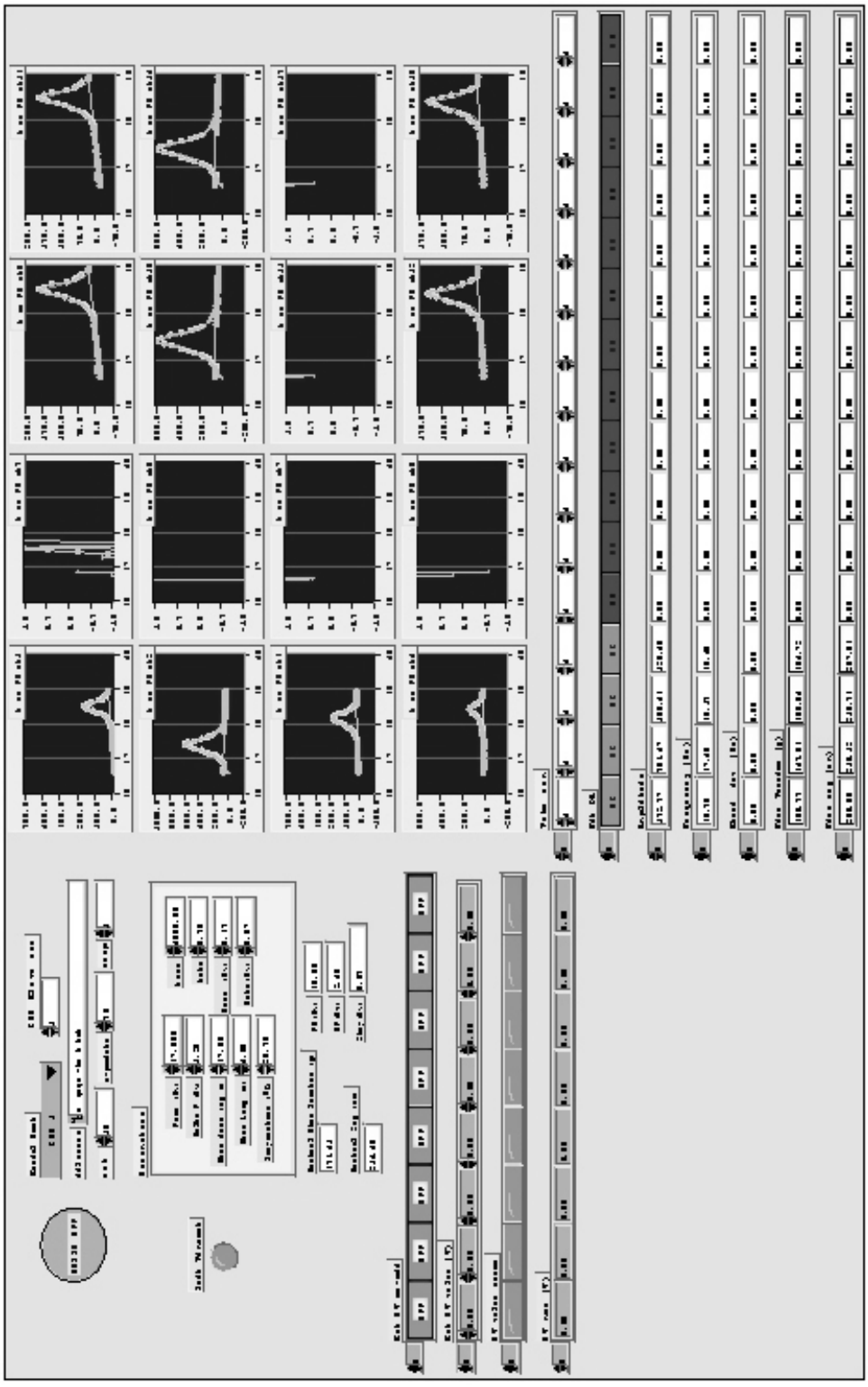

Figure 13: WTM LabVIEW control panel

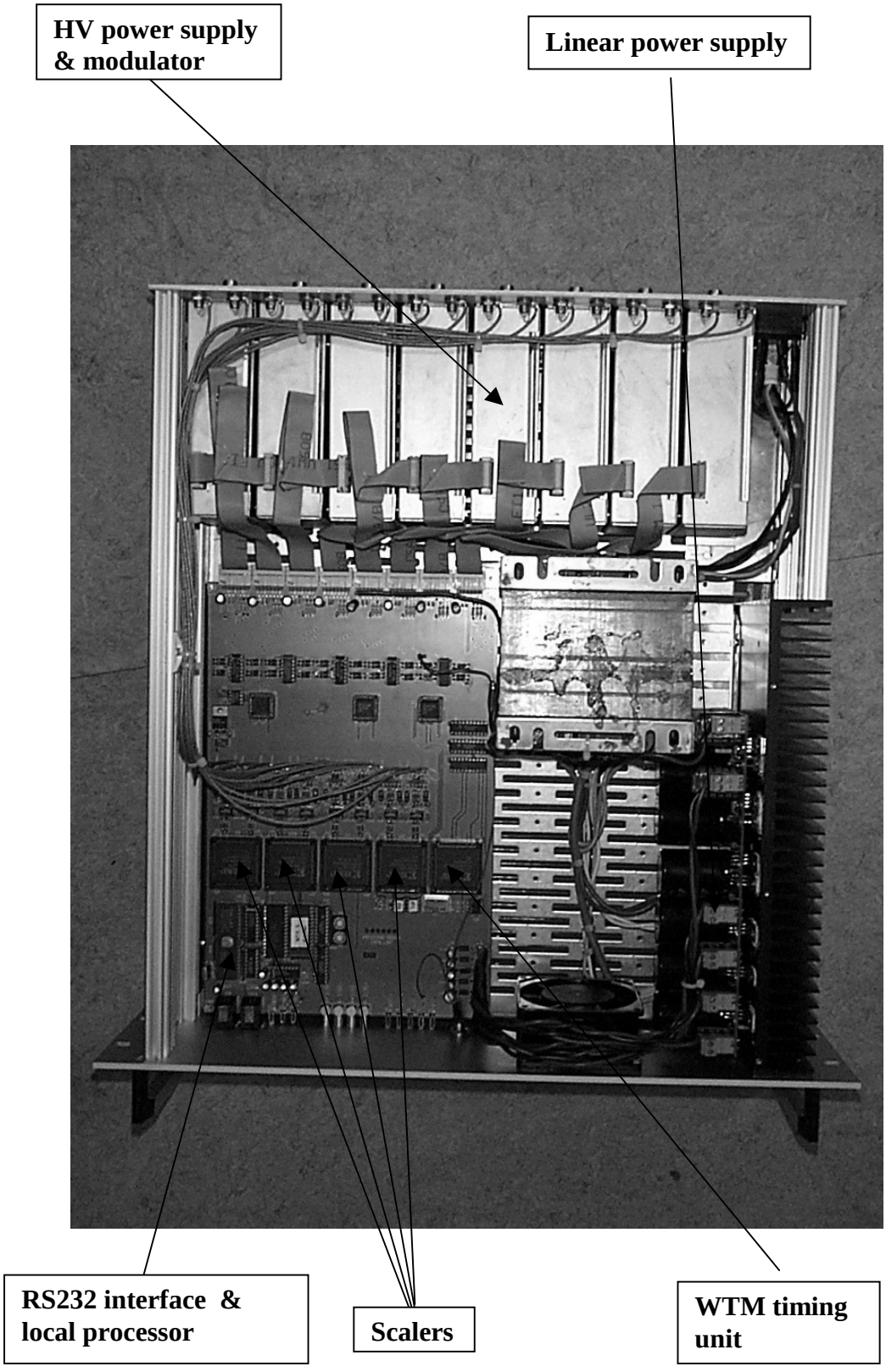

Figure 14 : WTM (internal view)

Figure 15 : Sixteen tube measurement setup

[1] STRINGING, CRIMPING AND RELATED TOPICS FOR KLOE DC. V. Kulikov, A. Nedosekin , 6/96 KLOE internal memo #60

[2] ELECTROSTATIC DIGITAL METHOD OF WIRE TENSION MEASUREMENT FOR KLOE DRIFT CHAMBER. A. Andryakov,…V. Kulikov, …A. Nedosekin, Nucl. Instrum. & Meth. A409:63-64,1998

[3] MDT wire tension measurement using an electrostatic method, ATLAS internal note ATL-MUON-38-264